STUDIES IN LOW POWER DIGITAL TELEMETRY AND DATA SYSTEMS

by

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To my Family

A C K N O W L E D G E M E N T S

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LIST OF PRINCIPAL SYMBOLS

$|H(\omega)|$ = modulus of $H(\omega)$

$\overline{n(t)}$ = the time average or ensemble average of $n(t)$

$\dot{x}(t)$ = derivative with respect to time of $x(t)$

$\underset{\sim}{x}$ = phasor representation of the variable x

x^* = complex conjugate of complex number x

A, A(t) = amplitude, amplitude response

Atten. = attenuation

a = real part of complex constant

a_c = filter attenuation parameter for optimum discriminator detection

a_p = dummy variable

α = real part of complex root

α_z = random phase angle

B = bandwidth in Hertz, constant amplitude

$B_k(s)$ = k - th order Bessel polynomial

B_ω = bandwidth in rads.s^{-1}

b = imaginary part of complex constant

b_c/

b_c = number of bit coincidences

β = imaginary part of complex root

C = channel capacity, capacitance

C_z = constant

D = normalised keying frequency separation

D_{opt} = optimum value of D

$D(s)$, $D_1(s)$ = polynomials in s with distinct complex roots

$d_n(t)$ = discriminator noise output signal

$d_o(t)$ = total discriminator output signal

d_1, d_2 = parameters defining error probability in envelope detection of FSK

$\Delta\omega_d$ = deviation between carrier and keying frequencies

$\Delta\omega_z$ = a small variation in ω_z

E_a = per-centage asymmetry in band-pass filter characteristic

e = electronic charge (1.6×10^{-19} coulomb)

e_a, e_c = error probability parameters

$e_o(t)$ = deterministic envelope response

erf(x)/

$\mathrm{erf}(x)$ = error function

$\mathrm{erfc}(x)$ = complementary error function

γ = normalised complex cross-correlation coefficient

F = Farad

$F(s)$ = Laplace transform with distinct complex poles

$F(\gamma, G)$ = generalised error probability for discriminator detection of FSK

f = frequency in Hertz, pulse rate

$f(t)$ = time dependent function

G = open-loop gain, filter constant, parameter in determining error probability

G_{opt} = optimum value of G

$g_c(t)$ = general cosine function

γ = average signal-to-noise power ratio

H = Henry

$H(s)$ = filter transfer function

I_o = modified Bessel function of zero order

i = current

j/

j = $(-1)^{\frac{1}{2}}$

K_d = discriminator sensitivity

K_f = feedback-control sensitivity

K_v = voltage-controlled oscillator sensitivity

K_1, K_2 = complex conjugate constants

k = variable denoting filter order

k_f = voltage-to-frequency transfer gain

k_p = voltage-to-phase transfer gain

L = inductance

$\mathcal{L}\{v(t)\} = V(s)$ = Laplace transform of $v(t)$

$\mathcal{L}^{-1}\{V(s)\} = v(t)$ = inverse Laplace transform of $V(s)$

λ = phase angle

M = mutual inductance, modulus of constants K_1 and K_2

m_c, m_{c3} = bandwidth/pulse-settling time products

N = mean noise power, noise power spectral density

$N(s)$, $N_1(s)$ = polynomials in s

n = number of binary-code bits per word

n_b = number of bits per balanced-code word

n_c /

n_c = number of prime channels per frame

$n(t)$ = band-limited Gaussian noise signal

Ω = ohms

ω = frequency in rads.s^{-1}

P_e = probability of error

P_{em} = probability of error with derived model of the PLLD

P_{eg} = generalised error probability for discriminator detection

$\Phi(t)$ = total excess-phase response

$\phi, \phi(t)$ = phase, phase function

$\psi, \psi(t)$ = phase, phase function

Q = Markum Q function, quality factor

q = subscript denoting quantised

R = resistance

$R(t)$ = total envelope response

r_c = cross-correlation coefficient between bit-patterns

r_k = complex roots of k-th order polynomial

$r(t)$ = total response

$r_{oc}(t), r_{os}(t)/$

$r_{oc}(t)$, $r_{os}(t)$ = deterministic cosine and sine responses

ρ_k = normalised complex roots of a k-th order polynomial

$Sa(x)$ = sampling function $\sin(x)/x$

S_r = average received signal power

s = complex frequency variable

s_n = normalised complex frequency variable

s_r = slope of the ramp test signal

σ = quantisation-step height

T = bit period

T_c = channel sampling period

T_i = interrogation pulse period

T_z = time period specified by the variable z

t = time

τ = time constant

θ, $\theta(t)$ = phase, phase function

$u(t)$ = Heaviside unit-step function

V = volts

V_{da} = D/A convertor feedback voltage

V_s/

V_s = dynamic range of the PCM encoder

V_{sh} = sample-and-hold voltage

V_r = reference voltage

v = voltage

$v(t)$ = deterministic signal function

$W_d(\omega)$ = average power spectral density of the balanced-code data signal

$W_s(\omega)$ = average power spectral density of the transmitted FSK signal

$W_n(\omega)$ = average noise power spectral density

$X(t)$ = Gaussian noise signal with possibly non-zero mean

$X_d(\omega)$ = spectrum of the balanced-code data signal

$X_s(\omega)$ = spectrum of the transmitted FSK signal

$x(t)$ = Gaussian noise signal with zero mean

$Y(t)$ = Gaussian noise signal with possible non-zero mean

$y(t)$ = Gaussian noise signal with zero mean

Z = impedance

S U M M A R Y

In recent years there has been an increasing requirement in the bio-medical field for multi-channel telemetry systems. The telemetry sources are required to be small, light in weight, and of low-power consumption. Recent advances in micro-electronics have made it possible to implement micro-power digital systems, thus (as far as the writer is aware), it has been possible for the first time to apply digital techniques to bio-telemetry. In particular, the present analysis is concerned with the application of such techniques to near-field bio-telemetry from an implanted source.

Of the possible transmission systems, PCM/continuous-wave FSK is shown to have the most suitable characteristics for these conditions. Discriminator detection of FSK is chosen to be the reception technique on the basis of an investigation of the performance of the feasible receiver systems. For test purposes, the transmitter source is implemented using available MSI and thin-film devices. The FSK detector is implemented using a phase-locked-loop frequency discriminator. Automatic frequency control is incorporated in the receiver to overcome conflicting bandwidth requirements and frequency stability. Inexpensive and unsophisticated bit- and frame-synchronisation systems have been developed for data recovery. The results obtained from experiments devised to test the operation of the telemetry system show good agreement with theoretical predictions and, moreover, define an operational threshold for the system.

INTRODUCTION

In the last decade much effort has been expended in the development of specialised electronic instrumentation which would allow quantitative physiological studies to be carried out on undisturbed subjects. Radio-telemetry, using progressively smaller electronic devices[1, 2, 3, 4, 5], was recognised as the most promising path towards a physiologically acceptable measurement environment in which there is no restriction to the normal movements of the living subject. More recently, systems for radio-telemetry from sources implanted within an animal body[4, 5, 6, 7] have been developed to facilitate measurements in situations where external wire attachments are unacceptable.

Understandably, because there is a legal as well as a physical limit to the volume of implantable material, the radio-telemetry systems vary in complexity according to the need to implant. Multi-channel FM/FM, FM/AM and PDM/FM systems are described in the literature[1, 2, 3, 4] for non-implanted telemetry sources, whilst simpler single-channel FM systems are reported[4, 5] for implanted sources. Whether the telemetry sources are implanted or not, however, there is a need for practicable multi-channel systems[6, 7]. (It is only by monitoring simultaneously the various measurable biological parameters that any possible correlations between parameters can be found.) The feasibility of a multi-channel digital telemetry system for the radio transmission of biological data from

a/

a source implanted within an experimental animal (the domestic fowl in particular) is considered in this thesis.

Digital systems have in the past been disregarded for the transmission of biological data because of their extreme network complexity, size and power consumption. Even now, an implantable digital telemetry source would be impracticable were it not for a recent achievement in the micro-electronics industry, viz. the development of a range[8] of COS/MOS (complementary-symmetry/metal-oxide-semiconductor) IC's, monolithic integrated circuits containing P- and N- channel MOS transistors. These digital IC's, featuring power dissipations of the order of 10μW for MSI (medium-scale-integration) circuits with a 10 Volt power supply, provide a basis for innovation in the field of telemetry from biological subjects. The involvement of micro-electronics firms in custom design and/or fabrication of complete systems as LSI (large-scale-integration) circuits provides further motivation for consideration of an implantable digital telemetry source, since the digital circuitry required could be produced as a single IC.

It seems likely, therefore, that the major difficulties of excessive power consumption and circuit size in a multi-channel digital telemetry system designed for bio-physical purposes can be overcome by realising an implantable large-scale-integration COS/MOS circuit. Specifically, this thesis deals with the studies involved in the development and evaluation of such a low-power radio-telemetry system as a precursor to the necessarily costly fabrication of LSI circuits.

CHAPTER 1

A DIGITAL BIO-TELEMETRY SYSTEM

1.1 A characterisation of telemetry systems

'Telemetry' has previously been defined[9] as the science of transmission of otherwise inaccessible data to accessible locations. 'Bio-telemetry', in particular, is defined as the science of transmission of otherwise inaccessible data from biological subjects to accessible locations. However, since the transmission of information/data can be accomplished by a variety of telemetry systems, these require some form of systematic characterisation.

Various modulation techniques[10, 11, 12, 13, 14] have been developed that increase the efficiency of a telemetry transmission medium by

(i) allowing a possible exchange of signal-to-noise power ratio for transmission bandwidth, and

(ii) allowing more than one information channel to be transmitted simultaneously by the same medium.

Consideration of these modulation techniques is, therefore, an useful first step in the characterisation of telemetry systems.

Several well-known modulation techniques are listed and grouped for system/

system characterisation in table 1.1.1. Two basic types of modulation system can be distinguished and characterised in terms of modern information theory[14]. These are

(i) analogue systems, which involve the transmission and detection of an infinite number of messages, and therefore waveforms, not all of which are known, and

(ii) digital systems, which involve the transmission and detection of a finite number of messages, and therefore waveforms, all of which are known.

Analogue systems fall into two groups, A.1 and A.2(say).Group A.1 consists of the continuous-wave modulation techniques AM, FM and PM. These modulation techniques are obtained by allowing the transmission signal parameters of amplitude, frequency and phase respectively to vary individually as direct analogues of an information signal or message waveform (considered to be continous-wave and band-limited in this text) which has an infinite number of possible values and therefore messages associated with it.

Group A.2 consists of the sampled-data modulation techniques PAM, PFM, PDM and PPM. These modulation techniques are based on the Sampling Theorem[10, 11, 12, 13]; according to which an information carrying signal can be recovered from a series of periodic samples of that signal, provided the sampling frequency is greater than or equal to twice the bandwidth of the original information signal. It should/

ANALOGUE SYSTEMS		DIGITAL SYSTEMS	
A.1	AM - Amplitude Modulation FM - Frequency Modulation PM - Phase Modulation	D.1	ASK - Amplitude-Shift Keying FSK - Frequency-Shift Keying PSK - Phase-Shift Keying
A.2	PAM - Pulse-Amplitude Modulation PFM - Pulse-Frequency Modulation PDM - Pulse-Duration Modulation PPM - Pulse-Position Modulation	D.2	QPAM (Q signifies 'quantised') QPFM QPDM QPPM
		D.3	PCM - Pulse-Code Modulation DM - Delta-Modulation (1-bit and n-bit coded) D-ΣM - Delta-Sigma Modulation (1-bit and n-bit coded)

Table 1.1.1

should be noted that this group of modulation techniques is essentially analogue in character, the pulse parameters of amplitude, frequency, duration and position, as the case may be, being varied individually as direct analogues of the information signal at the sampling instants.

In view of (ii) above, however, the implementation of a digital telemetry system (for the transmission of a continuous-wave information-carrying signal) requires some preliminary process for selecting a finite number of waveforms from the infinite available. This is achieved in practice by the 'quantisation' (loosely defined here as the approximation of a variable to the nearest of a set of allowed discrete values) of the information signal in both time and signal value, since both are required to define the information available. Accordingly, two groups of digital modulation techniques, D.1 and D.2 (say), are produced by similarly applying the process of quantisation to the analogue modulation techniques (discussed above) in both time and modulation-parameter value.

Group D.1 consists of the digital keying techniques ASK, FSK, and PSK obtained by thus quantising the continuous-wave modulation techniques of group A.1. The sampled-data systems of group A.2 are quantised in time through the periodicity of the sampling so that group D.2 consisting of QPAM, QPFM, QPDM, and QPPM, is obtained by simply quantising the relevant pulse-modulation parameters.

A/

A third group of digital modulation techniques D.3 comprises PCM,[10, 11, 12] DM (1-bit[16, 17] and n-bit coded[18]), and D-ΣM (1-bit[19] and n-bit coded). These techniques have better transmission properties than the quantised sampled data techniques of group D.2. As an indication of this, let us compare PCM and QPPM. Say 100 quantisation levels are required to give the required accuracy in the transmitted information signal, then the pulse period in QPPM is divided into at least 100 time intervals. On the other hand, if these levels were coded as in PCM, using two levels to represent the binary digits (bits) '1' and '0', then only seven time intervals, allowing 128 combinations of seven bits, would be required. If the same sampling period is used for both techniques, the transmission bandwidth[9, 10, 11, 12] (which is dependent upon the inverse of the time interval or bit period) is smaller by at least a factor of 10 when using PCM. The various quantised sampled-data systems referred to find application mainly as intermediate modulation stages in the generation of PCM and n-bit coded DM.

The concept of coding a fixed alphabet (i.e. a collection of allowed message symbols) for information transmission is not new. Probably the best known of all digital techniques is the keying of alpha-numeric data by means of morse code which appeared early in the history of electric telegraph systems.

So far, the modulation techniques have been considered for the transmission of information from a single source only. Most

telemetry/

telemetry systems, however, require to be multiplexed,[10,11,12] (i.e. designed so as to transmit more than one channel of information simultaneously). There are two basic techniques of multiplexing, viz. frequency-division multiplex (FDM) and time-division multiplex (TDM). Characterisation of telemetry systems will be incomplete, therefore, without consideration of these multiplexing techniques.

In FDM, the spectra of the various modulated signals occupy different bands in the frequency domain and can therefore be separated by appropriate filters. The signals to be transmitted are continuous and mixed in the time domain whilst maintaining their identity in the frequency domain. Signals in sampled-data and digital systems, on the other hand, are time-division multiplexed. Here, different signals occupy pre-determined distinct time slots, and can therefore be separated by appropriate switching. To make most efficient use of the frequency spectrum of the transmission medium, FDM and TDM sampled-data systems normally employ the continuous-wave analogue modulation techniques for transmission, whilst the digital systems normally employ the keying techniques listed above.

It is apparent that a great variety of telemetry systems are available to meet the requirements of a given information source and transmission medium. Definition of the type of telemetry system, appropriate in any context, either analogue or digital, is probably best achieved by considering the final receiver-end function. If an attempt is made to recognise a received signal as part of a finite alphabet of signals the system is considered to be digital. Alternatively, if

no/

no such attempt is made and the received signal is accepted at face value as a possible signal, the system is considered to be analogue. A receiver may in fact be asked to perform both tasks, in which case the telemetry system will be, in general, a hybrid analogue-digital system.

Digital telemetry systems, and in particular their application in the transmission of biological data, are considered in greater detail in the rest of this chapter.

1.2 Digital bio-telemetry

The design of a biological radio-telemetry system involves circuit design problems which arise from the wide variety of biological phenomena to be monitored and the necessity to investigate some of the various possible inter-relationships between these phenomena simultaneously. Specifically, the wide frequency and dynamic ranges involved in the measuring process make the task difficult. A generalised idea about the scope of the handled data[1, 6, 7] can be obtained by taking their extreme values.

The lowest frequencies encountered, viz. of order 0·1 to 0·2 Hz, are observed in the action of the heart and of the respiratory system. The clinically meaningful myoelectric potential frequency range extends up to 500 Hz, and in some problems frequencies as high as 5000 Hz are of interest. Electrical brain activity is characterised by/

by the lowest biological potential amplitudes, viz. voltages of order 10 μV, when picked up by external scalp electrodes. On the other hand, the greatest biological potentials result from muscle activity, and are of the order of a few millivolts.

Several of these biological signals can be transmitted simultaneously by using either TDM or FDM. From the practical point of view of implementing a biological telemetry system, however, TDM systems prove to have two[10] major advantages over FDM systems:-

(i) In FDM a different carrier is required to be generated for each channel at the transmitter source. Each channel occupies a different frequency band so that different band-pass filters need to be designed for the receiver end. TDM systems, on the other hand, require identical circuitry for each channel consisting of relatively simple analogue gates which are widely manufactured now as low-power IC's[8, 20]. Thus, for low power consumption and bulk size at the transmitter source, implementation of a TDM system has a very distinct advantage over the analogue circuits of modulators and carrier generators used in FDM systems.

(ii) TDM systems are less prone to inter-channel interference such as arises in FDM systems because of amplifier non-linearities in the transmission path[10]. The nonlinearity bounds for an FDM system are, therefore, more stringent than those for a single channel. In TDM systems the signals from different/

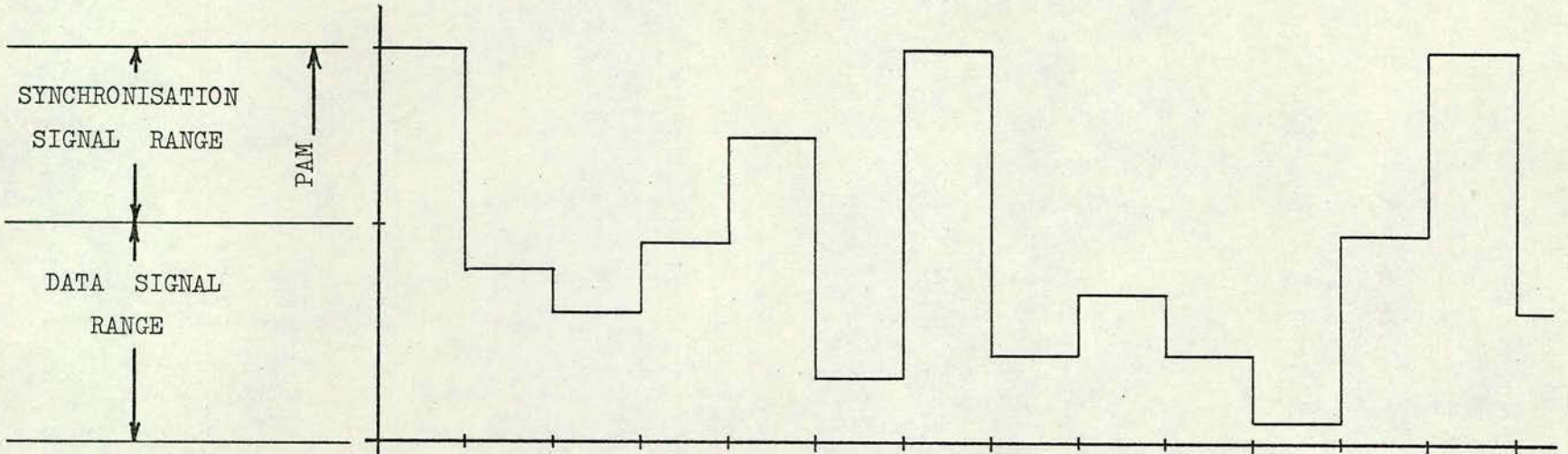
different channels are not applied simultaneously so that amplifier nonlinearity requirements are the same as those for a single channel.

TDM systems are also capable of efficiently accommodating the wide variety of frequency ranges associated with the various biological parameters. The structure of a typical TDM/PAM system is given in fig. 1.2.1 where five successive PAM samples are arranged serially, together with a sample level for receiver synchronisation purposes. These six channels define the basic group/frame structure of the TDM/PAM transmission system and are referred to here as prime channels. The structure of this TDM/PAM system is then described as a six-prime channel-per-frame system.

Supercommutation is used in TDM system to obtain higher sampling rates and therefore allows a higher frequency response on a few channels of information. This is implemented by arranging that an information signal should feed more than one prime-channel input, taking care (as shown in fig. 1.2.1) that the sampling period remains constant.

By using subcommutation techniques, on the other hand, many channels of slowly varying data can be handled at lower sampling rates. Subcommutation is accomplished by using one prime channel to define a subsystem in which successive PAM samples, together with a sample level for receiver synchronisation purposes, are arranged serially into a subframe (as shown in fig. 1.2.1) with a sampling rate equal to the prime channel sampling rate divided by the total number of subchannels per subframe.

Implementation/



CLASSIFICATION OF THE TDM/PAM SIGNAL CHANNELS													
SYNCHRONISATION CHANNELS	FS				SFS		FS						FS
PRIME DATA CHANNELS		P2		P4				P2		P4			
SUBCOMMUTATED DATA CHANNELS											S2		
SUPERCOMMUTATED DATA CHANNELS			SU			SU			SU			SU	

Fig. 1.2.1 The structure of a typical TDM/PAM system.

Implementation of subcommutation techniques is achieved at the expense of an increase in system complexity which involves mainly an increase in the number of analogue sampling gates. In view of (i) above, this is more acceptable in a biological system than the increase in the circuitry that would be required to accommodate more channels in an FDM system.

The practical attractions of a TDM system with either sampled-data or digital-coded modulation techniques are apparent. Also, since it now seems possible to overcome the practical drawbacks (viz. power consumption and bulk size) of implementing the coded PCM and n-bit DM systems by using a large-scale integration COS/MOS circuit, these digital coded systems can be considered in their own right as useful modulation techniques for bio-telemetry.

The theoretical usefulness of a modulation technique is measured in terms of the exchange between bandwidth and signal-to-noise ratio. The channel capacity (i.e. maximum rate of information transfer) in a channel contaminated with white Gaussian noise is, according to the Shannon-Hartley Law[14], given by

$$C = B \log_2 (1 + \gamma) \qquad \text{.....(1.2.1),}$$

where B is the channel noise bandwidth in Hz, and γ is the average signal-to-noise power ratio in the transmission channel.

By/

By applying eqn. (1.2.1) at the input and output of an ideal demodulator (which has the same channel capacity at both input and output) it follows that, when $\gamma_i \gg 1$ and $\gamma_o \gg 1$, then

$$\gamma_o \approx \left(\gamma_i\right)^{B_i/B_o} \qquad \text{.....(1.2.2),}$$

where the subscripts 'i' and 'o' indicate the input and output parameters respectively. The approximation (1.2.2) therefore represents the theoretically best exchange law between signal-to-noise power ratio and bandwidth.

The exchange law for digital-coded-modulation techniques is shown in the literature[10, 11, 12, 18, 19] to be of an exponential nature which compares favourably with the square-law exchange found in FM and PM[10, 11, 12], and the linear exchange occurring in PDM and PPM[13]. Accordingly, the implementation of a digital bio-telemetry system can be considered to have a sound theoretical, as well as a practical, basis.

The choice of an implantable digital bio-telemetry source is made (in the next two sections) by a consideration of the theoretical and practical aspects of

(i) the coded digital modulation techniques, and
(ii) the digital keying techniques which facilitate the radio transmission of digital information.

1.3 <u>The/</u>

1.3 The choice of a coded digital modulation technique (PCM)

A theoretical investigation of coded digital modulation techniques depends basically on characterising the effects of quantisation, since this is the common feature in these systems. A practical investigation, on the other hand, aims at exposing the basic characteristics and devising possible methods of implementing these techniques.

Quantisation has been defined (in sect. 1.1) as the process by which the infinite number of possible values of an analogue-modulated signal is reduced to a finite number of allowed possible values. As a result, an uncertainty is introduced into the transmitted value of the modulated signal which can never be removed. On reconstruction from the quantised signal, the original signal is obtained together with an error signal, described as quantisation noise[15].

Expressions indicating the relative noise suppression characteristics of the various coded digital modulation techniques, or more specifically formulae for their respective signal-to-quantisation-noise ratios, have been derived at various levels of complexity and for several signal inputs[10, 11, 12, 15, 18, 19]. The signal-to-quantisation-noise ratio (γ_q say) with a maximum amplitude non-saturating (full-load) sine-wave input signal is given here for PCM[18], n-bit DM,[18], and 1-bit D-ΣM[19], respectively, by the approximate/

approximate formulae

$$\gamma_q \approx \tfrac{3}{4}(f_s/f_m)(2^n - 1)^2 \qquad (n \geqslant 4) \qquad \text{.....(1.3.1),}$$

$$\gamma_q \approx \frac{3}{16\pi^2}(f_s/f_m)(f_s/f)^2(2^n - 1)^2 \qquad (n \geqslant 2) \qquad \text{.....(1.3.2),}$$

$$\gamma_q \approx \frac{3}{16\pi^2}(f_s/f_m)^3 \qquad \text{.....(1.3.3),}$$

where f_s is the signal sampling frequency, f_m is the maximum frequency of the information signal, f is the frequency of the sine-wave input signal, and n is the number of binary code bits.

It can be seen [from (1.3.1), (1.3.2) and (1.3.3)] that the noise suppression performance of both PCM and n-bit DM is significantly better than that of 1-bit D-ΣM and 1-bit DM. In view of this, and since no analysis could be found to describe the performance of n-bit D-ΣM, further discussion is limited, therefore, to PCM and n-bit DM.

The signal-to-quantisation-noise ratios defined by (1.3.1) and (1.3.2) are plotted in fig. 1.3.1 as functions of f_s/f_m in the case of n = 7 for sine-wave input signals of frequency $f = f_m/5$ and $f = f_m$. It can be seen that for PCM the γ_q vs f_s/f_m curve has a slope of 3dB per octave whilst the curves for DM have a slope of/

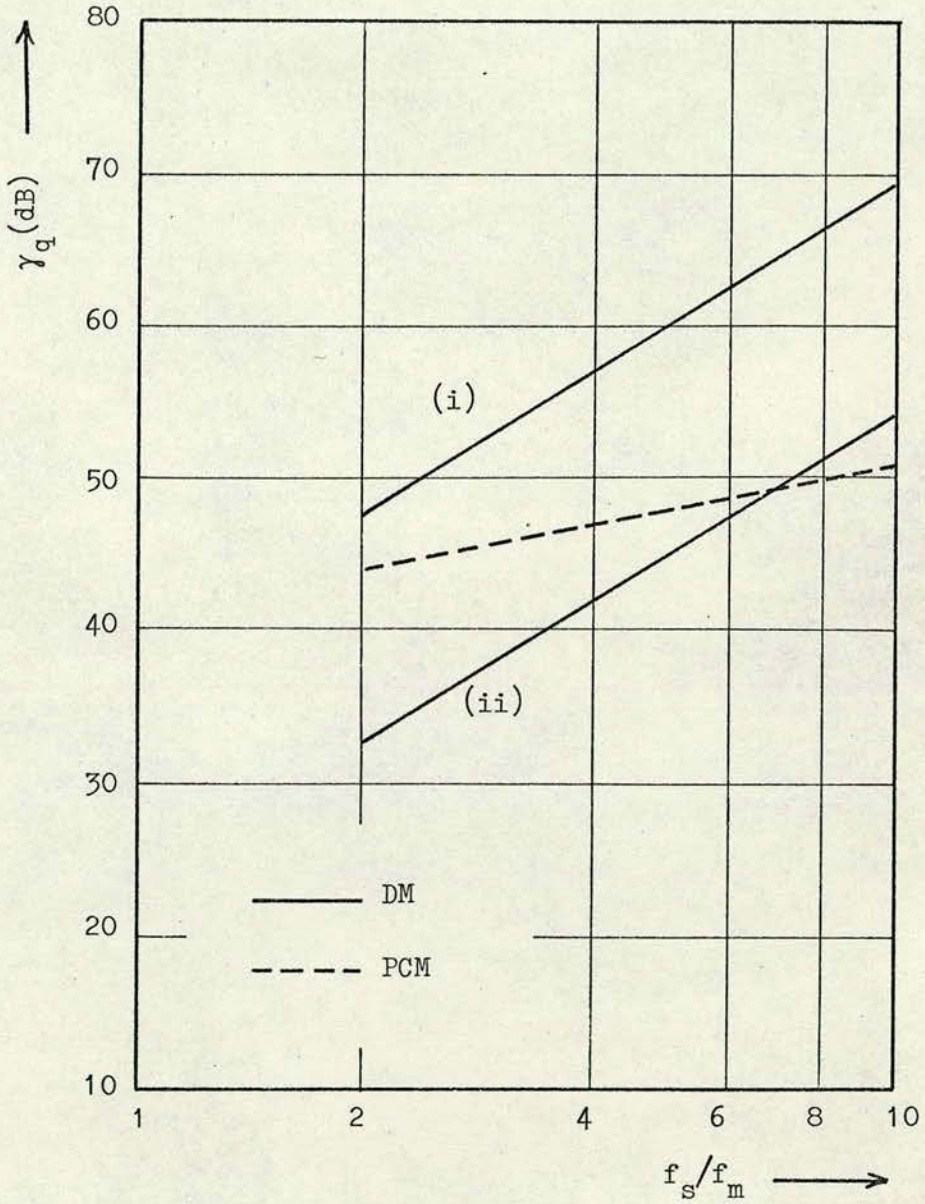


Fig. 1.3.1 Signal-to-quantisation-noise ratio γ_q as a function of f_s/f_m for 7-bit coded PCM and 7-bit coded DM with full-load sine-wave input signals of frequency (i) $f = f_m/5$ and (ii) $f = f_m$.

of 9dB per octave. At the lowest sampling frequency (that is $f_s/f_m = 2$), γ_q for DM is seen to be about 3dB better than that for PCM in the transmission of a full-load sine-wave signal with frequency $f = f_s/10$. According to (1.3.2), however, γ_q for DM is dependent on the sine-wave signal frequency. In the case of a sine-wave with signal frequency $f = f_s/2$, γ_q for PCM is then about 11dB better than that for DM. This figure is reduced at higher sampling frequencies (with a cross-over occurring at $f_s/f_m \approx 7$) as a result of the advantage in slope of 6dB per octave in favour of DM.

In view of these results, there is little to choose between the two modulation techniques at low sampling frequencies. A final choice between PCM and DM for the telemetry system being investigated is therefore made on consideration of the practical aspects of their basic characteristics and techniques of implementation.

The block diagrams of fig. 1.3.2 and 1.3.3 show the system requirements for the generation of multi-channel n-bit coded DM and PCM respectively. DM is generated by a method of quantised feedback. Information contained in the transmitted codes is mainly correlated to changes in the input signal and not simply to signal amplitude as is the case for PCM. An overloading of the DM system begins when the rate of change of the input signal reaches a certain limit. For a sine-wave of frequency f applied to the input of a DM system, the maximum amplitude (A_m say) which can be transmitted is given by[18]

A_m/

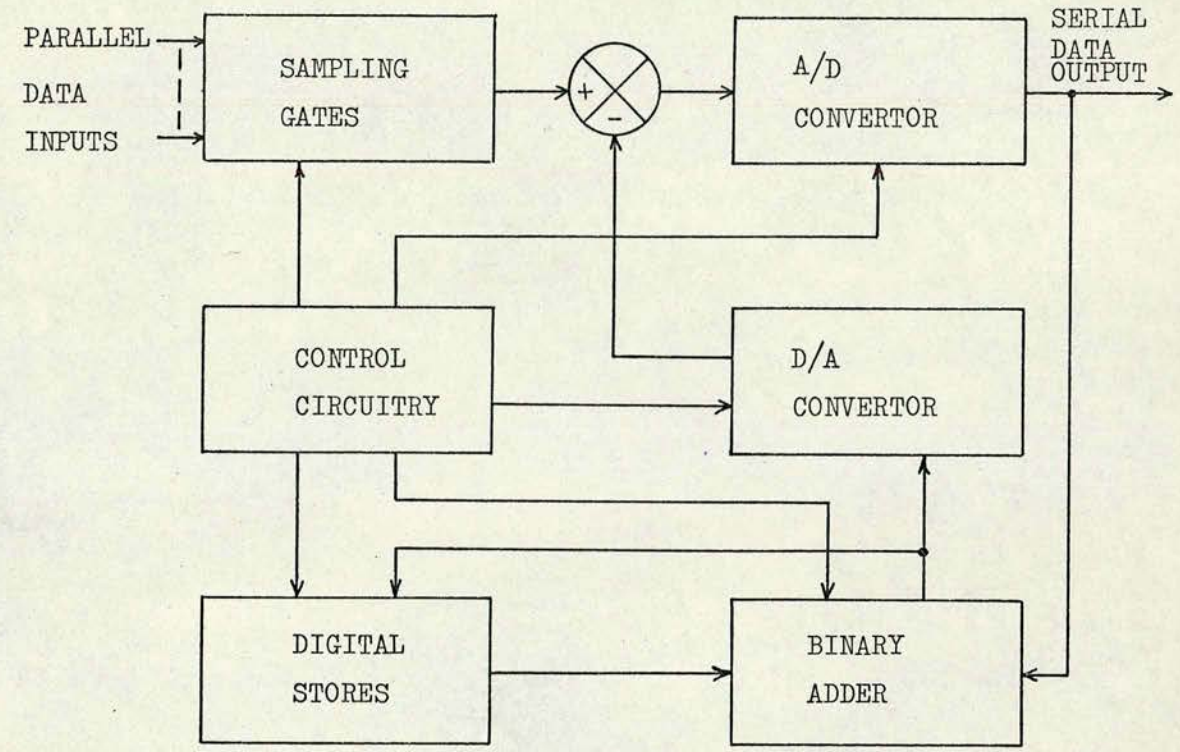


Fig. 1.3.2 Block diagram of a multi-channel n-bit DM system.

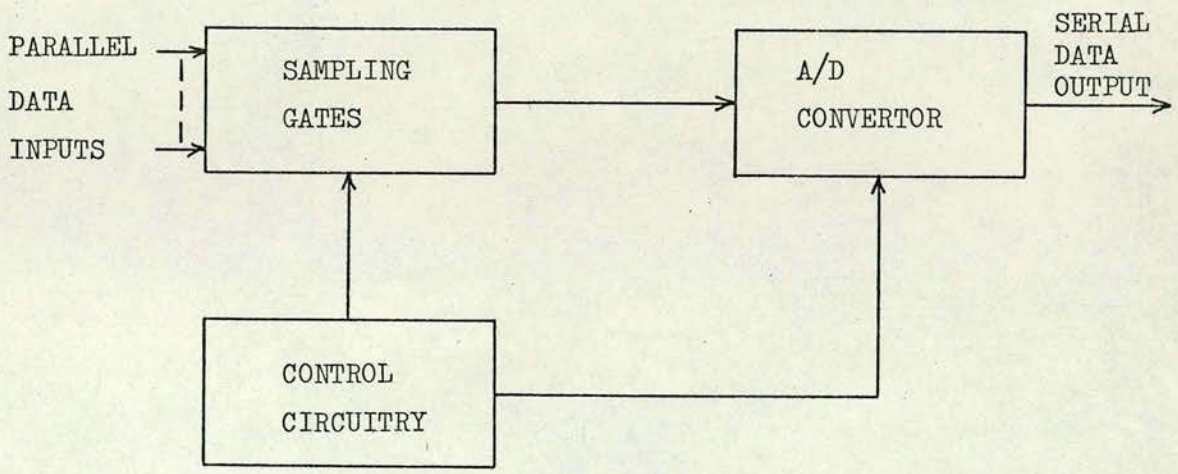


Fig. 1.3.3 Block diagram of a multi-channel PCM system.

$$A_m = (2^n - 1)\sigma f_s / 2\pi f \qquad \text{.....(1.3.4),}$$

where σ is the quantisation step height of the system analogue-to-digital (A/D) convertor. The corresponding maximum signal amplitude for PCM is given by[18]

$$A_m = (2^n - 1)\sigma / 2 \qquad \text{.....(1.3.5).}$$

For DM, it is seen [from eqn. (1.3.4)] that the maximum signal amplitude decreases with an increase in the signal frequency to be transmitted. DM is therefore well adapted to the transmission of signals (such as speech) which contain less energy in the higher frequencies than in the lower ones. However, since the spectra of various biological data sources are still being investigated, it must be postulated that a bio-telemetry system shall be capable of the transmission of signals with a constant spectrum in the band $(0, f_m)$. Accordingly, this raises serious design problems for the implementation of a DM system

Moreover, DM is particularly unsuitable for the transmission of zero frequency or slowly changing information (as will now be demonstrated). In a non-ideal channel there is (in addition to the quantisation noise) the normal random Gaussian noise. Quantisation and coding suppress the effects of this noise below a certain threshold value which will be one half the height of the transmitted pulses. Once this threshold is crossed, however, the random Gaussian noise causes an error in the decision of which bit is being transmitted. These errors/

These errors cause the wrong signal values to be decoded; thus effectively superimposing a random spurious signal component on the demodulated signal and quantisation noise. In PCM these spurious signals have no lasting effect. In DM, however, the integration[16,17,18] necessary in the receiver to reconstruct the information signal compounds the effects of the spurious signals and so corrupts the reconstructed signal permanently. This makes the transmission of low-frequency information signals by DM difficult to achieve.

It can be seen, by comparing figs. 1.3.2 and 1.3.3, that PCM also has a practical advantage over multi-bit DM in that it requires much simpler circuitry. (It should be noted here that, although the system is to be fabricated as an LSI circuit for implantation, there is still no justification in adopting unnecessarily complex techniques of implementation.) In view of these characteristics, the preferred digital modulation technique is PCM.

Having thus chosen the digital modulation technique to be implemented, the radio transmission system is considered next.

1.4 The choice of a digital keying technique (continuous-wave FSK)

The radio-frequency source will be modulated by a signal consisting of a series of PCM bits. Radio transmission of these digital signals is facilitated by the keying techniques of ASK, FSK, and PSK which differentiate between the finite number of modulating signal levels.

In/

In the case of binary signalling, two levels are required, corresponding to the binary digits '1' and '0'.

Since the system is essentially digital, the receiver function is to decide on the presence of one of a fixed number of possible signals. This decision will be made in the presence of additive random Gaussian noise, picked up by the antenna as antenna noise or as thermal noise in the radio-frequency (r.f.) amplifiers or mixer stages. This noise changes the transmitted signal characteristics[21] so that there is a possibility that the wrong signal will be chosen. For any digital reception system, this effect is characterised by a probability of error[10, 12] which depends upon the received signal-to-noise ratio.

Receiver filters are used to reduce the random noise power, but at the same time filter the high-frequency components in the pulse profile of the digital signal. It is necessary, therefore, to allow the detected digital signal to have reached a steady-state level before making a decision as to its value. To minimise bandwidth (and thereby reduce noise power) the reception decision is made at the end of each received pulse/bit period. [A receiver clock, locked to the received bit rate, decides the instant of decision and also supplies the timing information for the subsequent decoding of the separate channels of information.]

There are two basic types of receiver system for the detection of keyed digital information, viz. coherent and noncoherent. For

coherent/

coherent systems, there is assumed to be a signal available at the receiver which replicates the incoming signal in all respects. Coherent systems generally have lower error rates than non-coherent systems. [This should not be surprising, since more a priori information concerning the transmitted signal is available.]

Ideally, the keying technique which will allow the least overall probability of error should be chosen. The optimum P_e characteristics for several receiver systems have been described in the literature[10, 12, 22, 23, 24, 25]. Some of these are now given.

For ideal coherent detection of PSK,[12, 22, 23]

$$P_e = \tfrac{1}{2}\mathrm{erfc}(\sqrt{\gamma_r}) \qquad \ldots\ldots(1.4.1),$$

where erfc is the complementary error function, i.e.

$$\mathrm{erfc}(x) \equiv 1 - \mathrm{erf}(x) = \frac{2}{\sqrt{\pi}}\int_x^\infty \exp(-t^2)dt \qquad \ldots\ldots(1.4.2),$$

and γ_r is the signal-to-noise ratio in the receiver filter.

For ideal coherent 'dual-filter' detection of FSK[12, 22]

$$P_e = \tfrac{1}{2}\mathrm{erfc}\left\{\sqrt{(\gamma_r/2)}\right\} \qquad \ldots\ldots(1.4.3).$$

For ideal noncoherent 'dual-filter' detection of FSK,[12, 13, 22]

$$P_e = \tfrac{1}{2}\exp(-\gamma_r/2) \qquad \ldots\ldots(1.4.4).$$

For ideal coherent optimum threshold detection of ASK[12],

$$P_e = \tfrac{1}{2}\mathrm{erfc}(\tfrac{1}{2}\sqrt{\gamma_r}) \qquad \text{.....(1.4.5).}$$

For ideal noncoherent optimum threshold detection of ASK[12, 23]

$$P_e \approx \tfrac{1}{4}\mathrm{erfc}(\tfrac{1}{2}\sqrt{\gamma_r}) + \tfrac{1}{2}\exp(-\gamma_r/4) \qquad (\gamma_r > 1) \qquad \text{.....(1.4.6).}$$

These characteristics are plotted in fig. 1.4.1, where it becomes apparent that ideal coherent detection of PSK is the best of the detection techniques here considered.

Other factors for consideration in the choice of a suitable r.f. transmission technique, such as

(i) the r.f. system bandwidth requirements, and
(ii) the practical aspects of implementation in relation to the primary requirements of the telemetry system,

are of as much importance, in many systems, as the P_e characteristic. In the case of bio-telemetry systems, bandwidth and performance specifications have been laid down by the General Post Office[24]. These specifications limit low-power, near-field, telemetry devices, with a useful range of 1·5 metres, to the transmission band 300KHz to 30MHz so that transmission bandwidth does not present major problems. For implanted telemetry devices, it is the practical aspects of transmitter-end design/

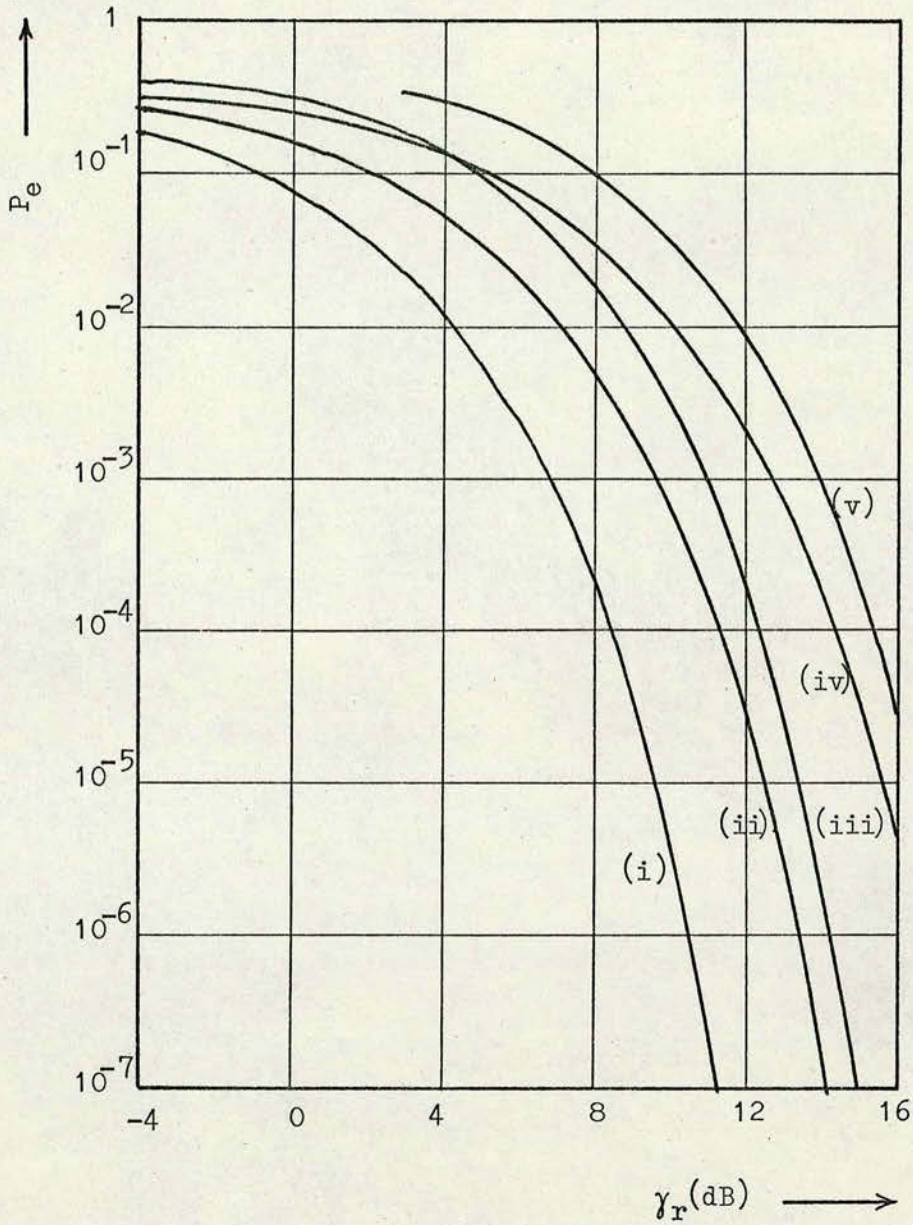


Fig. 1.4.1 Error probability P_e as a function of received signal-to-noise ratio γ_r for

(i) coherent PSK

(ii) coherent FSK ('dual-filter' detection),

(iii) non-coherent FSK ('dual-filter' detection),

(iv) optimum-threshold coherent ASK, and

(v) optimum-threshold non-coherent ASK.

design that are paramount.

The digital circuits of the TDM/PCM system can be comprised within an LSI circuit. However the circuits for r.f. transmission are essentially 'analogue'. Some circuits have previously been designed[5] and implemented using thin-film technology for implantation. It is proposed, therefore, that the complete transmitter end of the digital system being studied, should be finally constructed as an implantable hybrid LSI/thin-film micro-circuit.

Analogue circuits, even of a very simple nature, require large areas of thin-film and a significant amount of power consumption in a nominally 'low-power' system. By necessity, then, the r.f. oscillator/transmitter circuitry is very simple and therefore prone to drift and stability problems due to power-supply voltage and temperature changes.

Of the keying techniques, FSK is achieved most simply by allowing the digital PCM signal to vary continuously the bias on a varactor diode in an r.f. oscillator tank circuit. It is a moot point whether this system should be termed PCM/FSK or PCM/FM. For the purpose of this thesis, it will be considered as PCM/continuous-wave FSK since PCM/FM normally has some low-pass filtering of the PCM signal before r.f. modulation.

The familiar inter-relationship[9, 10, 11, 12] between FM and PM implies, however,

however, that the PCM/continuous-wave FSK system should not be considered in isolation. Specifically, a PCM/continuous-wave PSK system is achieved by first passing the PCM signal through a differentiation circuit at the input to the varactor diode. Since differentiation is approximated, in practice, by a simple resistor-capacitor R-C circuit which is readily implemented, these continuous-wave techniques of generating FSK and PSK are considered in detail.

Firstly, however, we investigate some useful FM relationships[9,10,11,12]. It is convenient to define a general angle-modulated signal

$$v_g(t) \equiv A \cos \theta_i(t) \qquad \text{.....(1.4.7)},$$

in which the amplitude A is constant. For a sinusoidal signal,

$$v_g(t) = A \cos(\omega_c t + \theta_o) \qquad \text{.....(1.4.8)},$$

simply, where here

$$\theta_i(t) \equiv \omega_c t + \theta_o \quad , \quad \omega_c \equiv d\theta_i(t)/dt \qquad \text{.....(1.4.9)},$$

and θ_o is a reference phase angle defined at time $t = 0$. If the frequency of an unmodulated carrier is ω_c (no distinction between angular frequency in $rad.s^{-1}$ or cyclic frequency in Hz is made in this thesis), the instantaneous frequency ω_i of a frequency-modulated carrier is given by

$$\omega_i(t) = \omega_c + k_f v_f(t) \qquad \text{.....(1.4.10)},$$

where/

where $v_f(t)$ is the modulating waveform, and k_f is the oscillator voltage-to-frequency conversion gain. The instantaneous phase $\theta_i(t)$ of the modulated carrier is the integral with respect to time of the instantaneous frequency, thus

$$\theta_i(t) = \omega_c t + \theta_o + k_f \int v_f(t)dt$$

$$= \omega_c t + \theta_o + k_p v_p(t) \qquad \text{.....(1.4.11),}$$

where

$$k_f \int v_f(t)dt \equiv k_p v_p(t) \quad \text{and} \quad k_f v_f(t) \equiv k_p dv_p(t)/dt \qquad \text{.....(1.4.12).}$$

The same signal can be regarded as a phase-modulated carrier with modulating waveform $v_p(t)$ and voltage-to-phase conversion gain k_p.

It should be noted that (1.4.12) defines the inter-relationship between FM and PM referred to above and substantiates the statement that PCM/continuous-wave PSK is achieved by first differentiating the PCM signal. Since PSK affords the best P_e characteristic (cf. fig.1.4.1), the PSK system making use of a simple R-C differentiation circuit is of particular interest and is now considered in detail.

If the PCM signal heights are defined as -V/2 and +V/2 volts, the response of a simple R-C differentiation circuit to transitions in the signal height occurring at t = 0 is given by

$v_f(t)/$

$$v_f(t) = a_p \exp(-t/RC) \qquad \text{.....(1.4.13),}$$

where $a_p \equiv +V$ and $a_p \equiv -V$ .....(1.4.14),

for a positive and negative transistion respectively. From eqns. (1.4.10) and (1.4.13) the instantaneous frequency becomes

$$\omega_i(t) = \omega_c + k_f a_p \exp(-t/RC) \qquad \text{.....(1.4.15).}$$

According to (1.4.11), the corresponding instantaneous phase angle is then

$$\theta_i(t) = \omega_c t + \theta_o + k_f a_p RC \left\{1 - \exp(-t/RC)\right\} \qquad \text{.....(1.4.16).}$$

By making the time-constant RC small, $\left\{1 - \exp(-t/RC)\right\}$ becomes a good approximation to a unit-step function. The depth of phase modulation is fixed by the value of $k_f a_p RC$. Unfortunately, however, the varactor diode (which is to be used for the voltage-to-frequency conversion) is a nonlinear voltage-dependent device. The two values of a_p [given in (1.4.14)] therefore define two corresponding values of k_f. In turn, this implies that the depth of phase modulation differs for positive and negative pulse transitions.

This method of implementing continuous-wave PSK therefore results in an unstable reference phase angle. In fact the reference phase angle either increases or decreases continuously (depending upon the value of k_f/

k_f associated with the positive or negative pulse transitions) as a function of the data to be transmitted. Data retrieval under these conditions is more complicated than for conventional PSK which has a stable reference phase angle.

We now consider the generation of continuous-wave FSK. In this application $v_f(t)$ is the PCM signal which implies [according to eqn. (1.4.10)] that $\omega_i(t)$ has only two values. Direct coupling (as apposed to capacitor coupling) of the PCM signal to the varactor diode ensures that the frequency-modulating waveform has two distinct voltage levels, which results in the desired keying of two distinct frequencies. It should be noted that capacitor coupling blocks the average value of the PCM signal (which by definition is data-dependent) so that the voltage levels of the waveform appearing at the varactor diode are in turn data-dependent. Capacitor coupling in situations where the average value of the PCM signal is unknown (or is likely to vary in an unknown manner) should therefore be avoided.

On balance having considered these simple continuous-wave techniques of generating PSK and FSK, the latter is preferred.

The choice of a digital bio-telemetry technique has now been made. Further consideration of this system requires a precise knowledge of the data transmission requirements.

1.5 The specification of a prototype transmitter source/

1.5 The specification of a prototype transmitter source

A multi-channel PCM/continuous-wave FSK system has been proposed as a digital telemetry system specifically for the low-power, near-field radio-transmission of several channels of biological information from an implanted source. The cost of fabricating the proposed transmitter source (viz. an implantable hybrid LSI/thin-film micro-circuit) can only be justified, however, after a detailed evaluation of the performance of a prototype transmitter source and telemetry receiver system.

To maintain as close a connection as possible with the proposed transmitter source, it was decided that the prototype should be built using, specifically, the medium-scale-integration COS/MOS devices available[8] and an existing thin-film oscillator circuit[5]. Since there is no definite limitation in the allowed transmission bandwidth (except that it should lie within the band 300kHz to 30MHz) and no practical limitation can be discussed at this stage, the only transmission requirement on the prototype transmitter source is that it should be capable of transmitting several channels of information with the highest expected range of frequency, viz. 500Hz. On the advice of a prospective user[25], it was decided that five data input channels with a minimum sampling frequency of 1000Hz and a signal resolution of one per cent of the signal dynamic range would meet that transmission requirement.

The/

The specification of a prototype telemetry receiver system is not made at this stage since (as is shown in the next chapter) several systems can be considered.

CHAPTER 2

THE CHOICE OF RECEIVER DETECTION TECHNIQUE

2.1 General

Two classes of receiver function (coherent and non-coherent) for the detection of digital keyed signals have been referred to in sect. 1.4. From fig. 1.4.1, which shows the relative performance of some detection systems in terms of their error probability, it can be seen that coherent detection is optimal for each of the keying techniques (viz. ASK, FSK and PSK) considered. Before choosing coherent detection on this basis, however, let us firstly consider the practical implications of its application in the detection of continuous-wave binary FSK, the keying technique proposed for this telemetry system.

Coherent detection of binary FSK is achieved by the direct comparison of two base-band message waveforms generated on multiplying the received signal with two receiver-based signals phase-locked to the two keying frequencies. In practice, the two receiver-based signals are generated by monitoring the received signal with two PLL's (phase-locked-loops) tuned separately to the two discrete keying frequencies. Since the noise component in the received signal produces a 'phase-jitter' in the phase-locked[26] output signals, which could effectively reduce the performance of the coherent detection technique/

technique, the PLL bandwidth is therefore reduced until an acceptably low-level of phase-jitter is obtained. As the speed at which normal PLL operation is then able to track variations in input-signal phase is reduced accordingly[26], practical coherent detection of binary FSK requires that the reference phase angles [cf. (1.4.8) above] associated with each frequency transmitted remain stable and unchanging except, possibly, for extremely slow drifts.

Theoretically, such a transmission characteristic may be obtained from a continuous-wave binary FSK source provided that the keying frequencies ω_1 and ω_2, and the bit-period T satisfy the relation[27, 28]

$$(\omega_2 - \omega_1)T = 2k\pi \qquad (\omega_2 > \omega_1) \qquad \text{.....(2.1.1)},$$

where k is an integer. To maintain this condition in practice, however, requires elaborate 'analogue' frequency-control circuitry. Since such circuitry cannot be implemented in a low-power, implantable transmitter source, and furthermore, since any change from the condition of (2.1.1) causes the reference phases associated with each keying frequency to be data-dependent (and are therefore not constant), the /to be continuous-wave binary FSK signal in this telemetry system is considered to be unsuitable for coherent detection.

Accordingly, the choice of receiver function is limited to the non-coherent detection techniques.

Two such techniques, viz.

(i) dual/

(i) dual filter envelope detection, and

(ii) discriminator detection,

are considered in detail in the remainder of this chapter.

2.2 'Dual-filter' envelope detection of binary FSK

A system block diagram[12] for the 'dual-filter' envelope detection of continuous-wave binary FSK is given in fig. 2.2.1. A series of binary pulses continuously modulate a carrier frequency which is then transmitted. At the receiver, this signal is passed, together with accumulated noise, through the system of band-pass filters and envelope detectors. The two envelope detector output signals are then compared, at a sampling instant synchronised with the original pulse train, and a decision is made on the presence or absence (as the case may be) of a particular binary digit according to which envelope-detector signal is the larger. Starting with a brief characterisation of the accumulated noise, we investigate the performance of this detection technique in this section.

There are various sources of noise which can be broadly classified as

(i) man-made noise such as might arise due to amplifier non-linearities causing distortion, or the pick-up of undesirable signals from other sources such as faulty contacts, electrical appliances, and ignition radiation;

(ii) random/

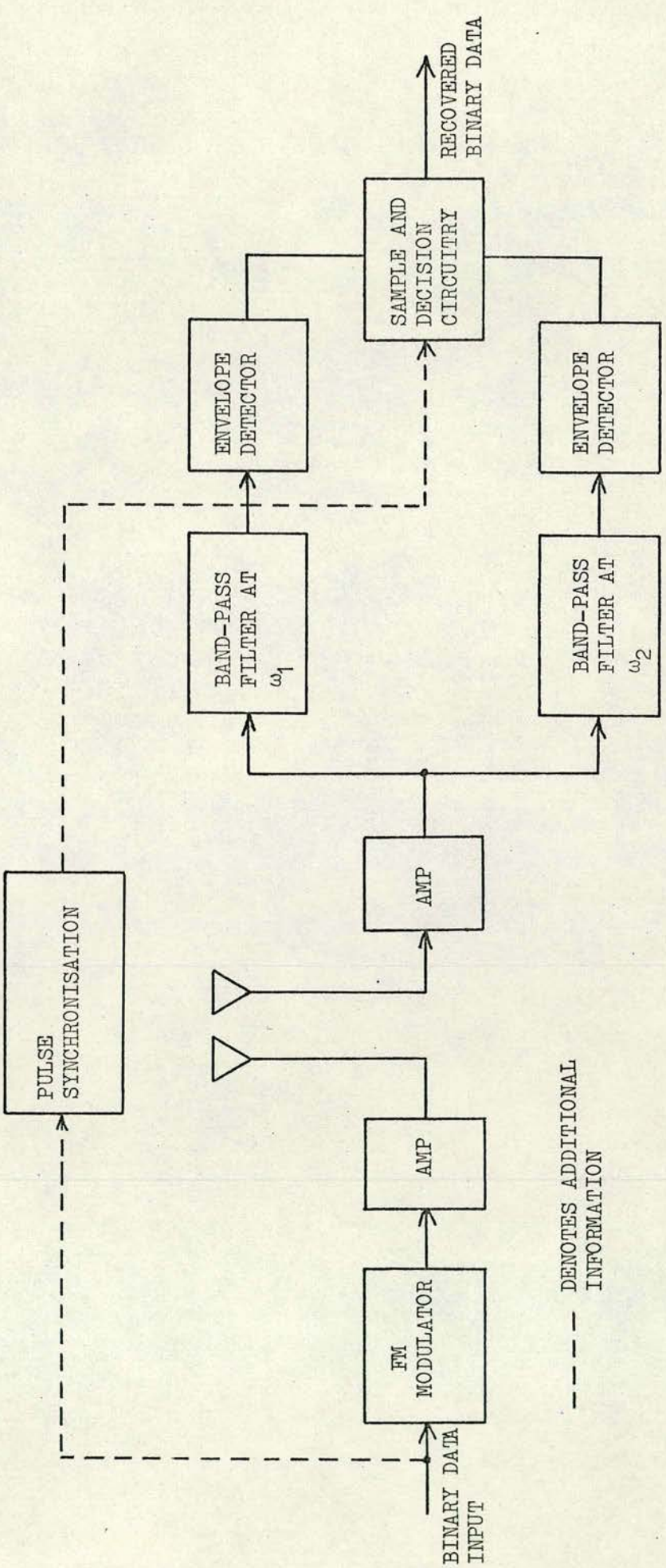


Fig. 2.2.1 Block diagram of the 'dual-filter' envelope detection system.

(ii) random natural disturbances such as the atmospheric noise picked-up in any telemetry process, and the thermal noise effects present in any electronic device.

For analysis purposes, however, it is assumed that noise corruption is due to the random processes of group (ii) [the distortion effects of group (i) are difficult, if not impossible, to predict] . Moreover, it is assumed that these processes produce a random noise signal which is wideband and has a constant power spectral density (a good approximation in the narrow-band situation to be considered here). This noise signal is then said to be Gaussian since its probability density function will have a Gaussian or normal distribution.

Rice[21] has shown that a band-limited Gaussian noise signal n(t) can be represented by the Fourier series

$$n(t) = \sum_z C_z \cos(\omega_z t - \alpha_z) \qquad \text{.....(2.2.1)},$$

where C_z depends on the band-limited properties of the noise defined by $W_n(\omega)$ (the noise-power spectral-density function) and has a constant value $\left\{2W_n(\omega_z)\Delta\omega_z\right\}^{\frac{1}{2}}$; α_z is assumed to be a random phase angle with a uniform probability distribution in the range $(-\pi, \pi)$; ω_z is defined by

$$\omega_z \equiv z\,\Delta\omega_z, \qquad \Delta\omega_z \equiv 2\pi/T_z \qquad \text{.....(2.2.2)},$$

so that in the limit, as $T_z \to \infty$ and $\Delta\omega_z \to d\omega_z$, the summation in eqn. (2.2.1) then becomes an integration. It is more convenient here,/

here, however, to manipulate the series representation.

It follows from eqn. (2.2.1) that

$$n(t) = \sum_z C_z \cos(\omega_z t - \omega_c t + \omega_c t - \alpha_z) \quad \text{.....(2.2.3),}$$

$$= x(t)\cos \omega_c t - y(t)\sin \omega_c t \quad \text{.....(2.2.4),}$$

where $$x(t) \equiv \sum_z C_z \cos \left\{ (\omega_z - \omega_c)t - \alpha_z \right\} \quad \text{.....(2.2.5),}$$

and $$y(t) \equiv \sum_z C_z \sin \left\{ (\omega_z - \omega_c)t - \alpha_z \right\} \quad \text{.....(2.2.6).}$$

x(t) and y(t) are seen to have exactly the same form as n(t), with all frequencies ω_z reduced by an amount ω_c. The statistical properties of x(t), y(t), and n(t) are therefore the same and may be summarised by[21]

$$\overline{x(t)} = \overline{y(t)} = \overline{n(t)} = 0, \quad \overline{x^2(t)} = \overline{y^2(t)} = \overline{n^2(t)} = NB \quad \text{.....(2.2.7),}$$

where N is the noise-power spectral density, B is the system equivalent noise bandwidth in Hertz, and $\overline{a(t)}$ denotes the ensemble average value of the function a(t). This representation of n(t) is particularly useful in band-pass filter systems in which ω_c can be considered to be the filter centre frequency, so that x(t) and y(t) are then effectively low-pass noise signals each having a power-density spectrum $W_n(\omega + \omega_c)$, where $W_n(\omega)$ is the power spectrum of n(t) defined by the band-pass filter. In this low-pass case, the noise bandwidths of x(t) and y(t) become B/2 and their noise power spectral densities become $2N$[21].

Accordingly,/

Accordingly, for the 'dual-filter' system considered here, with centre frequencies ω_1 and ω_2 corresponding to the same binary keying frequencies, the noise components $n_1(t)$ and $n_2(t)$ of the filter outputs may be represented in the form

$$n_1(t) = x_1(t)\cos\omega_1 t - y_1(t)\sin\omega_1 t \qquad \text{.....(2.2.8),}$$

and

$$n_2(t) = x_2(t)\cos\omega_2 t - y_2(t)\sin\omega_2 t \qquad \text{.....(2.2.9).}$$

The 'dual-filter' deterministic output signal components $v_1(t)$ and $v_2(t)$ can be similarly expressed[11,12]. Thus

$$v_1(t) = A_1(t)\cos\left\{\omega_1 t + \phi_1(t)\right\} \qquad \text{.....(2.2.10),}$$

$$= A_1(t)\cos\phi_1(t)\cos\omega_1 t - A_1(t)\sin\phi_1(t)\sin\omega_1 t \qquad \text{.....(2.2.11),}$$

and

$$v_2(t) = A_2(t)\cos\left\{\omega_2 t + \phi_2(t)\right\} \qquad \text{.....(2.2.12),}$$

$$= A_2(t)\cos\phi_2(t)\cos\omega_2 t - A_2(t)\sin\phi_2(t)\sin\omega_2 t \qquad \text{.....(2.2.13),}$$

where $A_1(t)$ and $A_2(t)$ are time-dependent amplitude response terms whilst $\phi_1(t)$ and $\phi_2(t)$ are time-dependent excess-phase (i.e. phase in excess of the carrier component) response terms respectively. The total 'dual-filter' output signals $r_1(t)$ $\left[= v_1(t) + n_1(t)\right]$ and $r_2(t)$ $\left[= v_2(t) + n_2(t)\right]$ then become

$$r_1(t) = \left\{A_1(t)\cos\phi_1(t) + x_1(t)\right\}\cos\omega_1 t - \left\{A_1\sin\phi_1(t) + y_1(t)\right\}\sin\omega_1 t \qquad \text{.....(2.2.14),}$$

$$= X_1/$$

$$= X_1(t)\cos \omega_1 t - Y_1(t)\sin \omega_1 t \qquad \text{.....(2.2.15)},$$

$$= R_1(t)\cos\{\omega_1 t + \Phi_1(t)\} \qquad \text{.....(2.2.16)},$$

$$\text{and } r_2(t) = \{A_2(t)\cos \phi_2(t) + x_2(t)\} \cos \omega_2 t - \{A_2 \sin \phi_2(t) + y_2(t)\} \sin \omega_2 t \qquad \text{.....(2.2.17)},$$

$$= X_2(t)\cos \omega_2 t - Y_2(t)\sin \omega_2 t \qquad \text{.....(2.2.18)},$$

$$= R_2(t)\cos \{\omega_2 t + \Phi_2(t)\} \qquad \text{.....(2.2.19)};$$

where

$$X_1(t) \equiv A_1(t)\cos \phi_1(t) + x_1(t) \qquad \text{.....(2.2.20)},$$

$$X_2(t) \equiv A_2(t)\cos \phi_2(t) + x_2(t) \qquad \text{.....(2.2.21)},$$

$$Y_1(t) \equiv A_1(t)\sin \phi_1(t) + y_1(t) \qquad \text{.....(2.2.22)},$$

$$Y_2(t) \equiv A_2(t)\sin \phi_2(t) + y_2(t) \qquad \text{.....(2.2.23)},$$

$$R_1^2(t) \equiv X_1^2(t) + Y_1^2(t) \qquad \text{.....(2.2.24)},$$

$$R_2^2(t) \equiv X_2^2(t) + Y_2^2(t) \qquad \text{.....(2.2.25)},$$

$$\tan \Phi_1(t) \equiv Y_1(t)/X_1(t) \qquad \text{.....(2.2.26)},$$

$$\text{and } \tan \Phi_2(t) \equiv Y_2(t)/X_2(t) \qquad \text{.....(2.2.27)}.$$

The functions $R_1(t)$ and $R_2(t)$, defined by (2.2.24) and (2.2.25) respectively, then represent the envelope-detector output signals which are compared at the sample-and-decision instants in order to establish/

establish the presence of a particular binary digit. From expressions (2.2.20) to (2.2.25), however, it can be seen that the functions $X_1(t)$, $X_2(t)$, $Y_1(t)$, and $Y_2(t)$, defining $R_1(t)$ and $R_2(t)$, are partly deterministic [in view of their dependence on the signals $A_1(t)$, $A_2(t)$, $\phi_1(t)$ and $\phi_2(t)$], and partly Gaussian [in view of their dependence on the noise signals $x_1(t)$, $x_2(t)$, $y_1(t)$ and $y_2(t)$] . Accordingly, the combined effect of these various signal components in $R_1(t)$ and $R_2(t)$ is to introduce an uncertainty in the decision making process, since errors occur when the noise signal components cause a larger output from the 'wrong' envelope detector at the sample-and-decision instant.

As demonstrated in sect. 1.4, the sample-and-decision process is made synchronously with the end of each bit period so as to minimise filter bandwidth (thereby reducing the received noise power), the filter bandwidth being chosen to allow the deterministic signal components in the filter output to attain a steady-state level before each sample-and-decision instant(thereby avoiding the effects of adjacent-bit interference). For this system, then, one bit period is allowed for the deterministic signals $v_1(t)$ and $v_2(t)$ in the filter outputs to attain a steady-state level in <u>both</u> amplitude and phase, as both variables appear in the expressions for $R_1(t)$ and $R_2(t)$ [cf. expressions (2.2.10) to (2.2.27)]. Accordingly, at the sample-and-decision instants the deterministic signal components in $X_1(t)$, $X_2(t)$, $Y_1(t)$ and $Y_2(t)$ can be considered to bias the Gaussian noise components. Hence for stationary noise, the statistics of $X_1(t)$,/

$X_1(t)$, $X_2(t)$, $Y_1(t)$ and $Y_2(t)$ are jointly Gaussian but possibly with non-zero means.

Having thus characterised the statistical properties of $X_1(t)$, $X_2(t)$, $Y_1(t)$ and $Y_2(t)$, then (in view of the error condition described above), the performance of this system may be specified in terms of an error-rate/error-probability characteristic. In particular, such an error-probability P_e characteristic is found by averaging over the ensemble statistics of $X_1(t)$, $X_2(t)$, $Y_1(t)$ and $Y_2(t)$ for the following error conditions, viz.

(i) $R_2(t) > R_1(t)$, when $R_2(t)$ represents the 'wrong' envelope detector output signal, and

(ii) $R_1(t) > R_2(t)$, when $R_1(t)$ represents the 'wrong' envelope detector output signal.

If the binary digits are transmitted with the same relative frequency (a good approximation in practice) then the probabilities $P(R_2 > R_1)$ and $P(R_1 > R_2)$ [denoting respectively the probability of occurrence of error conditions (i) and (ii)] are equal and may be combined so that

$$P_e = \tfrac{1}{2}P(R_1 > R_2) + \tfrac{1}{2}P(R_2 > R_1) \equiv P(R_1 > R_2) \quad \text{say} \qquad \text{.....(2.2.28).}$$

P_e was given previously in eqn. (1.4.4) for the ideal system[12]. This ideal system, however, is subject to certain unrealistic assumptions, viz./

viz.

(i) that adjacent-bit interference (such as might arise from filter transients, or imperfect synchronisation) does not occur,

(ii) that there is no external interference (such as might arise from the spectral sidebands of other signal sources),

(iii) that the additive random noise components at the outputs of the two filters are statistically independent and have equal spectral densities, and

(iv) that there is no cross-talk between filter outputs.

Stein[23] gives an expression for P_e in the more realistic case which includes the effects of adjacent-bit interference, cross-talk between the filter output signal components, and correlation between the filter output noise components. In the case of identical bandpass filters (which is normally an acceptable approximation) Stein's expression[23] for P_e, as defined by (2.2.28), reduces to

$$P_e = \tfrac{1}{2}\left\{1 - Q(\sqrt{d_2},\sqrt{d_1}) + Q(\sqrt{d_1},\sqrt{d_2})\right\} \qquad \text{.....(2.2.29),}$$

where Q is the 'Markum' Q function defined by

$$Q(m,n) \equiv \int_n^\infty \exp\left\{-\tfrac{1}{2}(m^2 + x^2)\right\} I_o(mx)x\,dx \qquad \text{.....(2.2.30)}$$

which/

which has the limiting properties

$$Q(m,o) = 1 \qquad \text{.....(2.2.31)},$$

whilst $Q(o,n) = \exp(-n^2/2)$ .....(2.2.32),

I_o signifying the modified Bessel function of zero order, and

$$\begin{matrix} d_1 \\ d_2 \end{matrix} \equiv \frac{1}{4NB} \quad \frac{A_1^2(t)+A_2^2(t)-4|\gamma|\sqrt{\{A_1(t)A_2(t)\}}\cos\{\Phi_2(t)-\Phi_1(t)+\phi_c\}}{1-|\gamma|^2}$$

$$\mp \frac{A_2^2(t) - A_1^2(t)}{\sqrt{(1-|\gamma|^2)}} \qquad \text{.....(2.2.33)},$$

in which[23] γ is the normalised complex cross-correlation coefficient between the filter output signals $r_1(t)$ and $r_2(t)$, and ϕ_c is the phase angle of γ.

To obtain the least error probability, the expression given in eqn. (2.2.28) must be minimised. By inspection, as $d_1 \to o$, so $Q(\sqrt{d_2},\sqrt{d_1}) \to 1$, and therefore $P_e \to \frac{1}{2}Q(\sqrt{d_1},\sqrt{d_2})$. The least value of P_e is obtained when $d_1 = o$, and then, in view of the limiting properties of (2.2.31) and (2.2.32),

$$P_e = \tfrac{1}{2}Q(o,\sqrt{d_2}) = \tfrac{1}{2}\exp(-\tfrac{1}{2}d_2) \qquad \text{.....(2.2.34)}$$

Minimisation of the error probability means, therefore, that the filter system/

system should be designed so that d_1 becomes as small as possible, whilst d_2 becomes as large as possible. From inspection of (2.2.33) the requirements are

(a) that $A_2(t)$ is maximised (i.e. the 'correct' deterministic amplitude function be allowed to reach its maximum/steady-state level at the time of decision),

(b) that $A_1(t) \rightarrow o$ (i.e. the 'wrong' deterministic amplitude function tends to zero), and

(c) that $|\rho| \rightarrow 0$.

Practically, requirement (a) is met by the choice of the minimum filter bandwidths discussed previously, whilst requirements (b) and (c) are both met by increasing the separation between the two keying frequencies[23].

If A_{2m} represents the maximum value of $A_2(t)$, as required by (a) above, then the limiting value of d_2 [obtained from (2.2.33) according to (a), (b) and (c) above] may be given by

$$d_2 = A_{2m}^2/2NB \qquad \text{.....(2.2.35).}$$

which essentially represents the received signal-to-noise power ratio γ_r. Substituting for $d_2 \equiv \gamma_r$ in eqn. (2.2.34) results in the idealised error-probability characteristic given by eqn. (1.4.4). Eqn (1.4.4) therefore describes (as might have been expected) the minimum attainable error probability for 'dual-filter' envelope detection of binary FSK.

Since/

Since receiver design aims at obtaining as low an error rate as possible for a given received signal-to-noise ratio, eqn. (1.4.4) is used later for comparison with the corresponding minimum error probability obtained for discriminator detection of binary FSK. The detection technique with the better error-reduction characteristic can then be chosen for implementation.

2.3 Discriminator detection of binary FSK

Fig. 2.3.1 illustrates the block diagram of a discriminator detection system for continuous-wave binary FSK. A sequence of binary pulses frequency modulates a carrier which is then transmitted. After transmission and reception, during which random noise is accumulated, the contaminated signal is passed first through a band-pass filter and then through a linear frequency discriminator which essentially gives a measure of the instantaneous frequency of the received signal. The discriminator output signal is sampled in synchronism with the original pulse train, and a decision, as to the presence of a particular binary digit, is then made according to whether the sample value is larger or smaller than the signal level known to represent the unmodulated carrier frequency.

For the purpose of analysis, it is assumed that the accumulated noise signal n(t) at the band-pass filter output is Gaussian (cf. sect. 2.2 above) and may be represented mathematically by eqn. (2.2.1).

We consider firstly the detection of an unmodulated carrier signal $v_u(t)$/

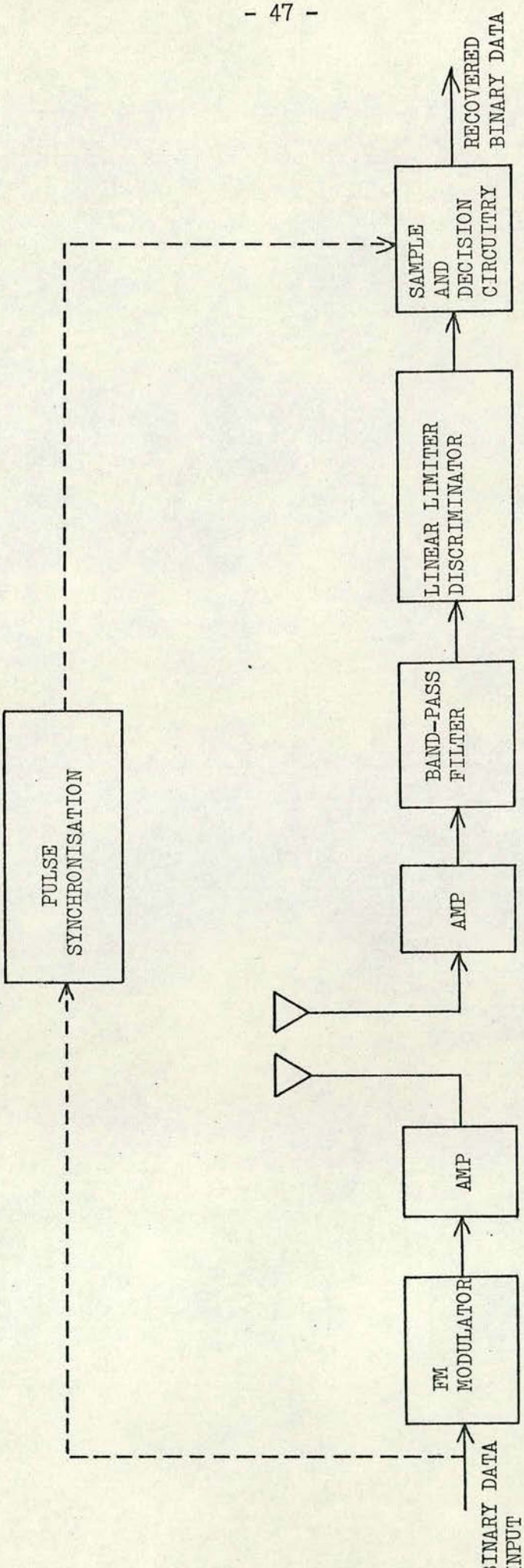


Fig. 2.3.1 Block diagram of the discriminator detection system.

$v_u(t)$ which is represented, according to the notation of (1.4.8), by

$$v_u(t) = A_u \cos(\omega_c t + \phi_u) \qquad \ldots\ldots(2.3.1),$$

where A_u is constant, ϕ_u is constant and the carrier frequency ω_c corresponds to the centre frequency of the band-pass filter. In this case, the deterministic signal at the filter output will be $v_u(t)$. It follows from eqn. (2.2.1) that the total filter output $r_u(t)$ $\left[= v_u(t) + n(t)\right]$ in this case can be written

$$r_u(t) = v_u(t) + \sum_z C_z \cos\left\{(\omega_z - \omega_c)t + \omega_c t + \phi_u - \alpha_z - \phi_u\right\} \ldots\ldots(2.3.2),$$

$$= A_u \cos(\omega_c t + \phi_u) + x_u(t) \cos(\omega_c t + \phi_u)$$

$$- y_u(t) \sin(\omega_c t + \phi_u) \qquad \ldots\ldots(2.3.3),$$

where $$x_u(t) \equiv \sum_z C_z \cos\left\{(\omega_z - \omega_c)t - \alpha_z - \phi_u\right\} \qquad \ldots\ldots(2.3.4),$$

and $$y_u(t) \equiv \sum_z C_z \sin\left\{(\omega_z - \omega_c)t - \alpha_z - \phi_u\right\} \qquad \ldots\ldots(2.3.5).$$

Eqn. (2.3.3) may be further reduced to

$$r_u(t) = \left\{A_u + x_u(t)\right\} \cos(\omega_c t + \phi_u) - y_u(t)\sin(\omega_c t + \phi_u) \qquad \ldots\ldots(2.3.6),$$

$$= R_u(t)\cos\left\{\omega_c t + \phi_u + \Phi_u(t)\right\} \qquad \ldots\ldots(2.3.7),$$

where $$R_u^2(t) \equiv \left\{A_u + x_u(t)\right\}^2 + y_u^2(t) \qquad \ldots\ldots(2.3.8),$$

and $$\tan \Phi_u(t) \equiv y_u(t) / \left\{A_u + x_u(t)\right\} \qquad \ldots\ldots(2.3.9).$$

If $r_u(t)$ is passed through first a limiter, to remove any unwanted amplitude variations, and then a balanced frequency discriminator with sensitivity K_d, the resulting output voltage $d_n(t)$ will be

$$d_n(t) = K_d\left\{\dot{\phi}_u + \dot{\phi}_u(t)\right\} \qquad \text{.....(2.3.10),}$$

where the dot signifies differentiation with respect to time. However, the phase angle ϕ_u is constant so that $\dot{\phi}_u = 0$, and $d_n(t)$ then becomes simply

$$d_n(t) = K_d\dot{\phi}_u(t) \qquad \text{.....(2.3.11),}$$

in which [from eqn. (2.3.9)] $\dot{\phi}_u(t)$ is given by

$$\dot{\phi}_u(t) = \frac{\left\{A_u + x_u(t)\right\}\dot{y}_u(t) - y_u(t)\dot{x}_u(t)}{\left\{A_u + x_u(t)\right\}^2 + y_u^2(t)} \qquad \text{.....(2.3.12).}$$

Since there is no deterministic carrier modulation, $d_n(t)$ is essentially a noise signal with zero mean in the balanced case considered here.

Now let us consider the detection of a continuous-wave binary FSK signal. In this case the deterministic signal $v_m(t)$ at the band-pass filter output is given by

$$v_m(t) = A_m(t)\cos\left\{\omega_c t + \phi_m(t)\right\} \qquad \text{.....(2.3.13)}$$

where/

where the time-dependent amplitude response function $A_m(t)$ and time-dependent excess-phase response function $\phi_m(t)$ represent the effect of band-pass filtering (with centre frequency ω_c) on the transmitted FSK signal. Following the analysis of the unmodulated case, the total filter output signal $r_m(t)$ $\left[= v_m(t) + n(t)\right]$ can be written

$$r_m(t) = v_m(t) + \sum_z C_z \cos\left\{(\omega_z - \omega_c)t + \omega_c t + \phi_m(t) - \alpha_z - \phi_m(t)\right\} \quad \ldots\ldots(2.3.14)$$

$$= A_m(t)\cos\left\{\omega_c t + \phi_m(t)\right\} + x_m(t)\cos\left\{\omega_c t + \phi_m(t)\right\}$$

$$- y_m(t)\sin\left\{\omega_c t + \phi_m(t)\right\} \quad \ldots\ldots(2.3.15),$$

where $$x_m(t) \equiv \sum_z C_z \cos\left\{(\omega_z - \omega_c)t - \alpha_z - \phi_m(t)\right\} \quad \ldots\ldots(2.3.16),$$

and $$y_m(t) \equiv \sum_z C_z \sin\left\{(\omega_z - \omega_c)t - \alpha_z - \phi_m(t)\right\} \quad \ldots\ldots(2.3.17).$$

Eqn. (2.3.15) may be further simplified to

$$r_m(t) = \left\{A_m(t) + x_m(t)\right\} \cos\left\{\omega_c t + \phi_m(t)\right\} - y_m(t)\sin\left\{\omega_c t + \phi_m(t)\right\} \quad \ldots\ldots(2.3.18)$$

$$= R_m(t) \cos\left\{\omega_c t + \phi_m(t) + \Phi_m(t)\right\} \quad \ldots\ldots(2.3.19),$$

where $$R_m^{\,2}(t) \equiv \left\{A_m(t) + x_m(t)\right\}^2 + y_m^{\,2}(t) \quad \ldots\ldots(2.3.20),$$

and $$\tan \Phi_m(t) \equiv y_m(t) / \left\{x_m(t) + A_m(t)\right\} \quad \ldots\ldots(2.3.21).$$

Accordingly,/

Accordingly, the output voltage $d_o(t)$ of the balanced frequency detector with sensitivity K_d is now given by

$$d_o(t) = K_d \left\{ \dot{\phi}_m(t) + \dot{\Phi}_m(t) \right\} \qquad \text{.....(2.3.22),}$$

in which [from eqn. (2.3.21)] $\dot{\Phi}_m(t)$ becomes

$$\dot{\Phi}_m(t) = \frac{\left\{ A_m(t) + x_m(t) \right\} \dot{y}_m(t) - y_m(t) \left\{ \dot{A}_m(t) + \dot{x}_m(t) \right\}}{\left\{ A_m(t) + x_m(t) \right\}^2 + y_m^2(t)} \qquad \text{.....(2.3.23).}$$

In the normal operation of the detection technique considered here, $d_o(t)$ is sampled in synchronism with the original pulse train and a decision on the presence of a particular binary digit is made according to whether $d_o(t)$ is positive or negative at the sampling instant. To avoid the effects of adjacent-bit interference, the deterministic signal components $\dot{\phi}_m(t)$, and $A_m(t)$, in $d_o(t)$ are allowed to reach a steady-state level before the sample-and-decision instant. As in 'dual-filter' envelope detection, the time allowed for all transient effects to cease is limited to one bit period (thus minimising filter bandwidth), the sample-and-decision instant being synchronised with the end of each bit period. From eqn. (2.3.22) the value of $d_o(t)$ at each sampling instant (t_s say) then becomes

$$d_o(t_s) = K_d \left\{ \Delta\omega_d(t_s) + \dot{\Phi}_m(t_s) \right\} \qquad \text{.....(2.3.24),}$$

where, for the received FSK signal, $\Delta\omega_d(t_s)$ $\left[\equiv \dot{\phi}_m(t_s) \right]$ represents the/

the deterministic steady-state frequency deviation from the carrier frequency ω_c at each sampling instant. Furthermore, since the steady-state level of $A_m(t)$ is given by $\dot{A}_m(t) = 0$, then it is simply shown [from eqn. (2.3.23)] that $\dot{\phi}_m(t_s)$ can be written

$$\dot{\phi}_m(t_s) = \frac{\left\{A_m(t_s) + x_m(t_s)\right\}\dot{y}_m(t_s) - y_m(t_s)\dot{x}_m(t_s)}{\left\{A_m(t_s) + x_m(t_s)\right\}^2 + y_m^2(t_s)} \qquad \text{.....(2.3.25).}$$

Comparison of eqns. (2.3.25) and (2.3.12) reveals that $\dot{\phi}_m(t_s)$ and $\dot{\phi}_u(t)$ are of the same form; the statistical properties of $\dot{\phi}_m(t_s)$ depend upon the statistical properties of $x_m(t_s)$, $\dot{x}_m(t_s)$, $y_m(t_s)$ and $\dot{y}_m(t_s)$, whilst the statistical properties of $\dot{\phi}_u(t)$ depend upon the statistical properties of $x_u(t)$, $\dot{x}_u(t)$, $y_u(t)$ and $\dot{y}_u(t)$. However, since the phase angle α_z [describing the noise signal n(t) in eqn. (2.2.1)] was originally assumed to be random with a uniform probability density function in the range $(-\pi, \pi)$, it follows that

(i) the statistical properties of $x_u(t)$ and $y_u(t)$ are independent of the value of the added phase component ϕ_u [cf. with (2.3.4) and (2.3.5)] and may therefore be summarised in the form of (2.2.7) by

$$\overline{x_u(t)} = \overline{y_u(t)} = \overline{n(t)} = 0, \quad \overline{x_u^2(t)} = \overline{y_u^2(t)} = \overline{n^2(t)} = NB$$

and .....(2.3.26),

(ii) the statistical properties of $x_m(t_s)$ and $y_m(t_s)$ are independent of the value of the phase component $\phi_m(t)$ added at each sampling instant/

instant t_s [cf. with (2.3.16) and (2.3.17)] and may therefore be summarised in the form of (2.2.7) by

$$\overline{x_m(t_s)} = \overline{y_m(t_s)} = \overline{n(t_s)} = 0, \quad \overline{x_m^2(t_s)} = \overline{y_m^2(t_s)} = \overline{n(t_s)} = NB \qquad \text{.....(2.3.27)}$$

Accordingly, the statistical properties of $\dot{\phi}_m(t_s)$ and $\dot{\phi}_u(t)$ are the same and eqn. (2.3.24) may be rewritten as

$$d_o(t_s) = K_d \Delta\omega_d(t_s) + K_d \dot{\phi}_u(t_s) \qquad \text{.....(2.3.28),}$$

which becomes

$$d_o(t_s) = K_d \Delta\omega_d(t_s) + d_n(t_s) \qquad \text{.....(2.3.29),}$$

where $d_n(t_s) \equiv K_d \dot{\phi}_u(t_s)$. [Eqn. (2.3.11) refers.]

At the sample-and-decision instants, then, the deterministic signal component in $d_o(t_s)$ [viz. $K_d \Delta\omega_d(t_s)$] can be considered to bias a noise component of zero mean [viz. $d_n(t_s)$]. This noise component introduces an uncertainty in the decision-making process since errors occur in the balanced detector output when $d_o(t_s)$ has a different sign from that of the deterministic signal component. The error-probability P_e is therefore found by averaging over the ensemble statistics of $d_o(t_s)$ for the error condition

$$\text{sgn}\left\{d_o(t_s)\right\} = -\text{sgn}\left\{\Delta\omega_d(t_s)\right\} \qquad \text{.....(2.3.30),}$$

so that

$$P_e = P\left[\text{sgn}\left\{d_o(t_s)\right\} = -\text{sgn}\left\{\Delta\omega_d(t_s)\right\}\right] \qquad \text{.....(2.3.31).}$$

Rice[21] has derived the ensemble statistics of $\dot{\phi}_u(t)$, and through these, the ensemble statistics of $d_n(t)$. Of particular interest is the probability density function $p\left\{d_n(t)\right\}$ [represented in ref. 21 by eqn. (5.4)], since the error probability for discriminator detection of binary FSK may be found by integrating $p\left\{d_n(t_s)\right\}$ over the region of incorrect decision defined by eqn. (2.3.30).

Curves of $p\left\{d_n(t_s)\right\}$ integrated over the appropriate region have been published by Meyerhoff and Mazer[29], and are reproduced here as fig. 2.3.2. These curves are of the generalised error probability $P_{eg} = F(\gamma_d, G)$ in which γ_d is the signal-to-noise ratio at the limiter input, and G is a function proportional to the frequency separation between the two keying frequencies. Specifically

$$G \equiv 2\Delta\omega_d\sqrt{(B/B_s)} \qquad \text{.....(2.3.32),}$$

$$\text{where} \quad B \equiv \frac{1}{2\pi}\int_0^\infty \left|H(\omega)\right|^2 \, d\omega \qquad \text{.....(2.3.33),}$$

$$\text{and} \quad B_s \equiv \frac{1}{2\pi}\int_0^\infty \left|H(\omega)\right|^2(\omega - \omega_c)^2 d\omega \qquad \text{.....(2.3.34),}$$

in which $\left|H(\omega)\right|^2$ is the band-pass-filter power characteristic and is the same as $W_n(\omega)$ which defines the noise signal n(t) (cf. sect. 2.2 above). It should be noted that B is the band-pass equivalent noise bandwidth in Hertz whilst B_s represents the second moment of $\left|H(\omega)\right|^2$ about the band-pass centre frequency ω_c.

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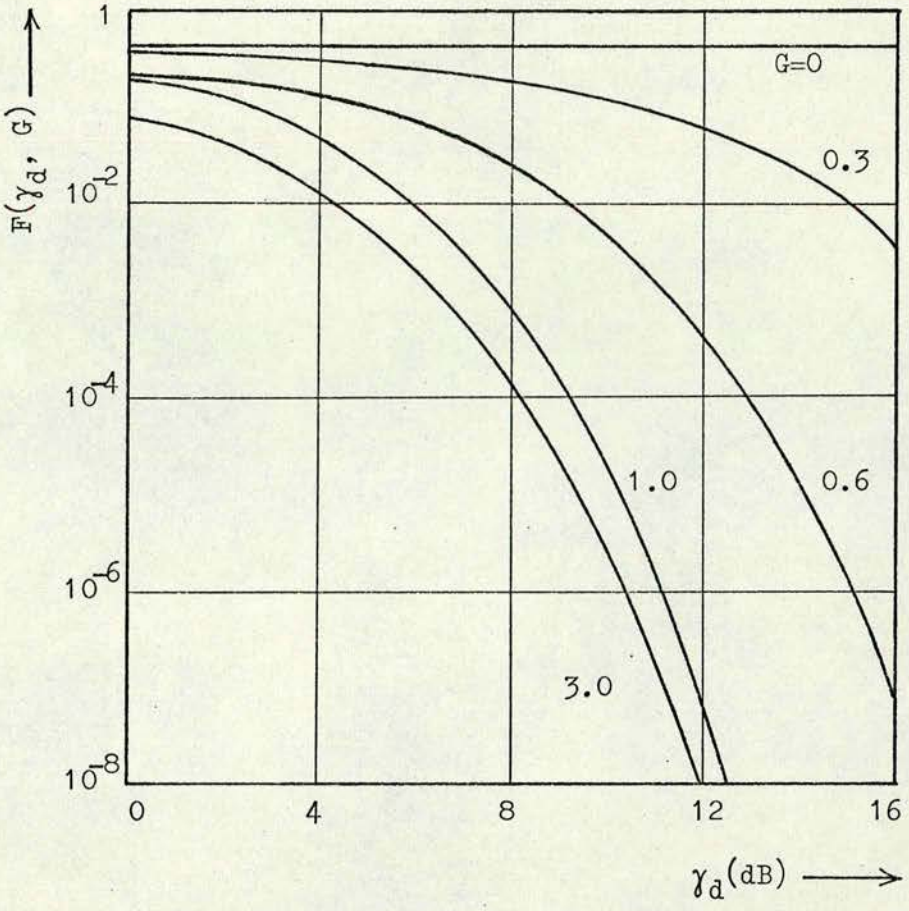


Fig. 2.3.2 Computed curves of $F(\gamma_d, G)$.

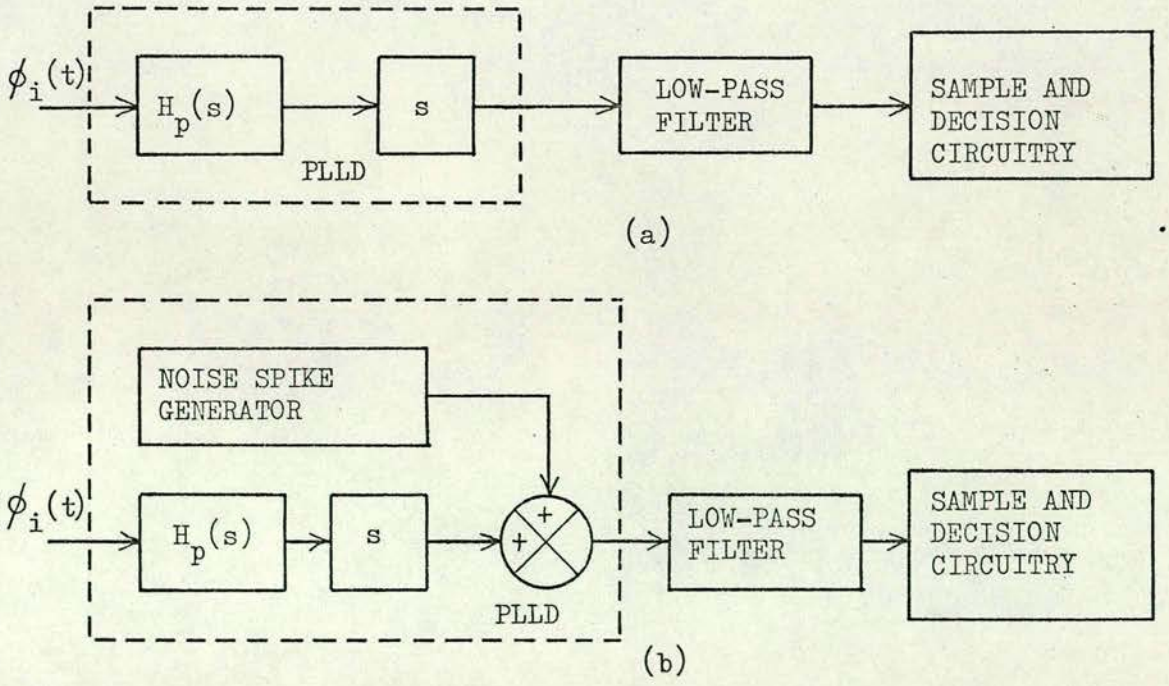


Fig. 2.3.3 Base-band models of the PLLD for
(a) large values of received signal-to-noise ratio, and
(b) low values of received signal-to-noise ratio.

This analysis has led to the generalised error-probability for ideal discriminator detection of binary FSK. It is well known, however, that all practical discriminators have a threshold input signal-to-noise ratio below which their operation departs noticeably from the ideal. In particular, a threshold level of around 10dB is reported[30] for simple discriminators, although this level may be reduced by the use of FM feedback[31, 32, 33, 34, 35] or a phase-locked-loop discriminator (PLLD)[33,36,37]. In view of the recent development in PLL integrated-circuit devices[38] which afford much simpler circuit design, the PLLD is to be preferred in practice, and its performance is considered accordingly.

At high input signal-to-noise ratios, the PLLD performs as an ideal discriminator and the base-band model for FSK detection can be represented as in fig. 2.3.3a. The PLLD input-phase signal $\phi_i(t)$ is given by

$$\phi_i(t) = \phi_m(t) + \int \phi_m(t) \qquad \text{.....(2.3.35),}$$

which is the excess-phase component of the modulated-carrier signal given by eqn. (2.3.19). Provided that the filtering effects of the PLL transfer function[26] $H_p(s)$ (s being the complex frequency variable) and the post-detection low-pass filter are negligible in comparison to the effects of the receiver band-pass filter, then the signal appearing at the decision-making unit will be essentially $\dot{\phi}_i(t)$, which is the signal analysed by Meyerhoff and Mazer[29].

At/

At low signal-to-noise ratios, the model of fig. 2.3.3a becomes inaccurate as the PLLD begins to lose and regain lock, thereby causing large bursts of noise in the discriminator output. If the PLLD falls out of lock about $\phi_i = 0$, then it regains lock about $\phi_i = \pm 2k\pi$ (k is an integer). In a broad-band loop, this phase change can be approximated as a step function [35, 36, 39, 40, 41] of amplitude $\pm 2k\pi$. The time derivative of phase (as seen at the demodulator output) is then either a positive or negative impulse of area $2k\pi$. Accordingly, an approximation to the PLLD in the threshold region is obtained (as shown in fig. 2.3.3b) by a dependent noise-spike generator added to the output of the base-band model of fig. 2.3.3a. The occurrence of these noise spikes is (to a good approximation) governed by Poisson statistics[35, 43, 44] provided that the ratio of the PLLD capture range to lock range is approximately unity[26, 35].

Using the model of the PLLD given in fig. 2.3.3b, Gagliardi[44] has adapted the generalised error-probability P_{eg} (obtained by Meyerhoff and Mazer[29]) to include the effects of the noise-spike generator.

Thus,

$$P_{em} = P_{eg}\exp(-\lambda) + \left\{1 - \exp(-\lambda)\right\} \qquad \text{.....(2.3.36),}$$

where P_{em} is the probability of error for the derived model of the discriminator, and

$\lambda \equiv$ /

$$\lambda \equiv \sqrt{(B_s/B)}\ \ln(2\pi B_d/\Delta\omega_d)\exp(-\pi^2\,\gamma_r/4)/2\pi B_d \quad \text{.....(2.3.37)},$$

where B_d is the bandwidth of the post-detection filter and γ_r is the received signal-to-noise power ratio. According to Gagliardi[44], the effects of the noise-spike generator are not apparent above γ_r = 4dB. This figure for the PLLD threshold supports the values obtained by other authors[35,37].

The generalised error-probability $\left[P_{eg} = F(\gamma_d, G)\right]$ derived for ideal discriminator detection of binary FSK therefore holds for practical systems provided that $\gamma_r > 4$dB. Further analysis to find the minimum error probability, however, requires a detailed knowledge of the system band-pass filter characteristics. Shaft[45] has derived the minimum error-probability for discriminator detection with an ideal Gaussian magnitude filter. The remainder of this chapter is concerned with an investigation of the error probabilities in practical filter systems.

2.4 Filters for pulse transmission systems

Pulse transmission systems require (among other things) filters whose impulse responses are (a) free from ringing and overshoot and (b) symmetrical about the time for which the response is a maximum. These characteristics are of importance since they tend

(i) to minimise the system 'bandwidth/pulse-settling-time product', which is the determining factor in the Gaussian noise reduction properties of such filter systems,

(ii) to reduce the adjacent-bit interference level found in pulse-filter systems of finite bandwidth, and

(iii) to allow the most efficient trade off between the above two seemingly incompatible requirements[46, 47].

The filter which satisfies the properties (a) and (b) above is known as a Gaussian filter. Essentially, the Gaussian filter provides the best approximation to a matched filter for pulse systems. Three types of filter approximate the ideal Gaussian filter, viz

(1) the Gaussian magnitude filter,

(2) the maximally-flat group-delay filter, and

(3) the equi-ripple group-delay filter.

Since these filters are approximations, there will always be some overshoot and asymmetry in the impulse response, the levels of which can, in general, be reduced by increasing the order of the approximation.

To show the effects of approximation on FSK-detector error probability, the maximally-flat group-delay filter, also known as the Bessel[46, 47] (or Thomson[48]) filter, was chosen since this filter was found to be widely documented in the literature. The Bessel filter approximating a linear phase characteristic with unity slope in the frequency domain has a low-pass transfer function given by[46]

$$H_{1k}(s) = G_{1k}/B_k(s) = G_{1k}/\prod_{x=1}^{k}(s - r_{1x}) \qquad \text{.....(2.4.1)},$$

where/

where $B_k(s)$ is a kth order Bessel polynomial in s (the complex frequency variable), G_{1k} is a constant normally defined to give zero attenuation at zero frequency, r_{1x} are complex roots of $B_k(s)$ which are either negative real or distinct complex-conjugate pairs[47].

Particularly in the communications field, it is often more convenient to define the filter characteristics of eqn. (2.4.1) in terms of a characteristic formalised with respect to a unity-3dB bandwidth[46]. Specifically, if ω_k defines the 3dB point of a kth order filter in eqn. (2.4.1), then a normalised complex frequency variable s_n can be defined such that

$$s_n = s/\omega_k \qquad \text{.....(2.4.2).}$$

Values of ω_k are listed in table 2.4.1 for several Bessel filters. From eqn. (2.4.1) the low-pass transfer functions with unity-3dB bandwidth are then given by

$$H_{1k}(s_n) = G_{1k}/B_k(\omega_k s_n) = G_{1k}/\omega_k^k \prod_{x=1}^{k}(s_n - \rho_{1x}) \qquad \text{.....(2.4.3),}$$

where $$\rho_{1x} \equiv r_{1x}/\omega_k \qquad \text{.....(2.4.4).}$$

For the FSK system being studied, the analogous Bessel band-pass filter is required. In this context, the effects discussed earlier refer to the envelope and excess-phase response functions of the received signal. Transformation from a low-pass to band-pass filter is accomplished by substituting for s_n, in eqn. (2.4.3), the expression

$s_n/$

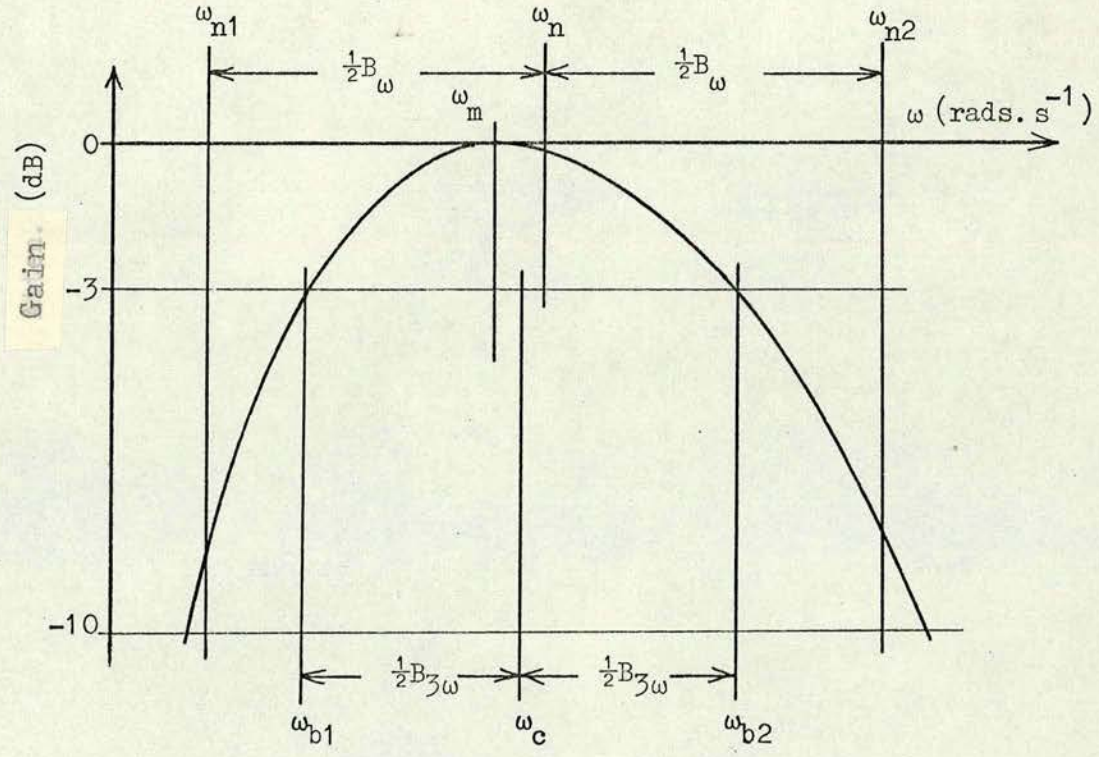


Fig. 2.4.1 Portrayal of the asymmetrical band-pass filter characteristic

k	3	4	5	6
ω_k	1.753	2.11	2.424	2.698

Table 2.4.1

k = 4	$\omega_c/B_{3\omega}$	10	20	30
	E_a	0.43	0.24	0.15

Table 2.4.2

$\frac{\omega_c}{B_{3\omega}} = 30$	k	3	4	5	6
	E_a	0.21	0.15	0.14	0.13

Table 2.4.3

he equivalent-area rectangle of height $|H_b(\omega)|^2_{max}$ is positioned so that mall lateral displacements of its vertical sides about their chosen positions have negligible effect in relation to $\int|H_b(\omega)|^2 d\omega$. This determines suitable choice for ω_{n_1} and ω_{n_2}; whence $\omega_n = \frac{1}{2}(\omega_{n2} + \omega_{n1})$ also $B_\omega = \frac{1}{2}(\omega_{n2} - \omega_{n1})$

$$s_n \equiv (s^2 + \omega_m^2)/B_{3\omega}s \qquad \text{.....(2.4.5)},$$

where $$\omega_m \equiv \sqrt{(\omega_{b1}\omega_{b2})}, \qquad B_{3\omega} \equiv \omega_{b2} - \omega_{b1} \qquad \text{.....(2.4.6)},$$

in which ω_{b1} and ω_{b2} define the band-pass 3dB points, and the filter centre frequency ω_c is then given by

$$\omega_c = (\omega_{b1} + \omega_{b2})/2 \qquad \text{.....(2.4.7)}.$$

The resulting band-pass filter transfer function $H_{bk}(s)$ becomes

$$H_{bk}(s) = G_{lk}(s\,B_{3\omega}/\omega_k)^k \Big/ \prod_{x=1}^{k}(s^2 - s\rho_{lx}B_{3\omega} + \omega_m^2) \qquad \text{.....(2.4.8)},$$

which is of the form

$$H_{bk}(s) = G_{bk}s^k \Big/ \prod_{x=1}^{k}(s - \rho_{bx})(s - \rho^*_{bx}) \qquad \text{.....(2.4.9)},$$

where $$G_{bk} \equiv G_{lk}(B_{3\omega}/\omega_k)^k \qquad \text{.....(2.4.10)},$$

and ρ_{bx}, together with its complex-conjugate ρ^*_{bx}, are distinct roots of the denominator polynomial in $H_{bk}(s)$.

The band-pass transformation formula of eqn. (2.4.5) is non-linear, and thus produces an asymmetrical band-pass characteristic. This effect is illustrated in fig. 2.4.1. For certain applications, and in particular for the FSK detection systems being considered in this chapter, a symmetrical band-pass characteristic is required. However, the asymmetry can be reduced to acceptable proportions by increasing the/

the ratio of $\omega_c/B_{3\omega}$ and also by increasing the filter order k.

A numerical integration program (described in appendix 1) was developed specifically for investigating the properties of band-pass filters. Of particular interest here are the filter parameters ω_{n1} and ω_{n2} which define the lower and upper limits of the noise equivalent band-pass filter. (Fig. 2.4.1 refers.) These two parameters define the filter noise equivalent bandwidth B_ω in radians such that

$$B_\omega = \omega_{n2} - \omega_{n1} \qquad \text{.....(2.4.11)},$$

and the filter noise equivalent centre frequency ω_n such that

$$\omega_n = (\omega_{n2} + \omega_{n1})/2 \qquad \text{.....(2.4.12)}.$$

Accordingly, a measure of the filter asymmetry is obtained from the values of ω_n and ω_c, and can be expressed as a percentage of B_ω; thus

$$E_a = 100(\omega_n - \omega_c)/B_\omega \qquad \text{.....(2.4.13)},$$

where E_a is the percentage asymmetry in the noise bandwidth. Examples of the computed results are given in tables 2.4.2 and 2.4.3. Table 2.4.2 shows the values of E_a obtained for various values of $\omega_c/B_{3\omega}$ in the case of a fourth-order (k = 4) Bessel filter. Table 2.4.3, on the other hand, shows the values of E_a obtained for various values of filter order k in the case of $\omega_c/B_{3\omega} = 30$. ~~In general,~~ It is found that for band-pass Bessel filters having $k \geqslant 2$ and $\omega_c/B_{3\omega} \geqslant 10$, the percentage/

percentage asymmetry in filter noise bandwidth is less than one per cent and is considered to be negligible accordingly.

With this information, the error probabilities in discriminator detection can now be investigated for a range of practical filters.

2.5 Minimum error probability in discriminator detection of binary FSK

The procedure for finding the minimum error probability in discriminator detection of FSK follows that given by Meyerhoff and Mazer in their derivation of the error probability in PCM/FM[29]. For comparison with other detection techniques, the curves of $F(\gamma_d, G)$ given in fig. 2.3.2 must be replotted as a function of γ_r (the received signal-to-noise ratio), the ratio γ_d/γ_r representing the reduction in signal power due to the filtering of the binary FSK frequencies by the narrow band-pass filter. Since G is dependent on the FSK frequency separation [cf. eqn. (2.3.31)] the value of $G(G_{opt}$ say) which minimises the function $F(\gamma_r, G)$, moreover, defines the optimum FSK frequency separation and gives for the minimum error probability

$$P_e = F(\gamma_r, G_{opt}) \qquad \text{.....(2.5.1).}$$

The principal task, then, is to derive the dependence of G and γ_d/γ_r on the frequency separation for a given realisable filter.

Several realisable filters were considered here, these being

(i) a/

(i) a range of Bessel band-pass filters [denoted by BFk (k = 3 to 6), where k is the filter order as defined in sect. 2.4 above] , and

(ii) the simple, critically-coupled tuned circuit (denoted by CCT) whose equivalent low-pass transfer function $H_{lt}(s_n)$ with unity-3dB bandwidth is given by

$$H_{lt}(s_n) = 1/(s_n^2 + \sqrt{2}s_n + 1) \qquad \text{.....(2.5.2)}$$

$$= 1/\left\{s_n + \frac{1}{\sqrt{2}}(1 + j1)\right\}\left\{s_n + \frac{1}{\sqrt{2}}(1 - j1)\right\} \qquad \text{....(2.5.3).}$$

The corresponding band-pass transfer function $H_{bt}(s)$ is obtained from eqn. (2.5.2) by substituting for s_n, according to (2.4.5), so that

$$H_{bt}(s) = \frac{(sB_{3\omega})^2}{s^4 + \sqrt{2}B_{3\omega}s^3 + (2\omega_m^2 + B_{3\omega}^2)s^2 + \sqrt{2}B_{3\omega}\omega_m^2 s + \omega_m^4} \qquad \text{.....(2.5.4),}$$

which is of the form[46]

$$H_{bt}(s) = \frac{G_{bt}s^2}{(s - \rho_{b1})(s - \rho_{b1}^*)(s - \rho_{b2})(s - \rho_{b2}^*)} \qquad \text{.....(2.5.5),}$$

where

$$G_{bt} \equiv B_{3\omega}^2 \qquad \text{.....(2.5.6),}$$

and the denominator polynomial of $H_{bt}(s)$ has distinct complex-conjugate pairs of roots viz. ρ_{b1}, ρ_{b1}^*, ρ_{b2} and ρ_{b2}^*.

It follows from (2.3.32) that G may be represented as

$$G = \pi(2\Delta f_d/B_3)\sqrt{(C_1/C_2)} \qquad \text{.....(2.5.7),}$$

$$= \pi D \sqrt{(C_1/C_2)} \qquad \text{.....(2.5.8),}$$

where $$D \equiv 2\Delta f_d/B_3 \qquad \text{.....(2.5.9),}$$

$$C_1 \equiv B/B_3, \text{and } C_2 \equiv B_s/B_3^3 \qquad \text{.....(2.5.10).}$$

The value of $\pi\sqrt{(C_1/C_2)}$ therefore defines the linear dependence of G on the normalised FSK frequency separation D for a given filter. The values of C_1 and C_2 were calculated numerically (with the aid of the computer program described in appendix 1) for the range of filters defined in (i) and (ii) above. These results together with the corresponding values of $\sqrt{(C_1/C_2)}$ and G/D are listed in table 2.5.1.

Variations in γ_d/γ_r as a function of D are determined, on the other hand, by the filter attenuation characteristics which are well documented for the filters being considered[46, 47, 48, 49].

For each band-pass filter, therefore, there are associated with each value of G corresponding values of D and γ_d/γ_r. The curves of $F(\gamma_d, G)$ given in fig. 2.3.2 can be shifted to the right by the value of γ_d/γ_r in dB to obtain $F(\gamma_r, G)$. Some of these shifts, together with the corresponding values of G, are listed in table 2.5.2 for the filters considered. The resulting curves for $F(\gamma_r, G)$ in the case of a fourth-order Bessel filter are given in fig. 2.5.1.

To/

FILTER TYPE*	C_1	C_2	$\sqrt{(C_1/C_2)}$	G/D
BF3	1.075	8.64	0.353	1.11
BF4	1.048	7.08	0.385	1.21
BF5	1.040	6.66	0.395	1.24
BF6	1.040	6.60	0.397	1.245
CCT	1.111	10.95	0.319	1.00

Table 2.5.1

	FILTER TYPE*									
	BF3		BF4		BF5		BF6		CCT	
	γ_d/γ_r		γ_d/γ_r		γ_d/γ_r		γ_d/γ_r		γ_d/γ_r	
G	ratio	dB (-)	ratio	dB (-)	ratio	dB (-)	ratio	dB (-)	ratio	dB (-)
1.5	0.292	5.35	0.326	4.9	0.348	4.6	0.354	4.5	0.165	7.8
1.2	0.443	3.5	0.504	3.0	0.525	2.8	0.533	2.75	0.325	4.9
1.1	0.511	2.9	0.571	2.45	0.59	2.3	0.593	2.25	0.405	3.9
1.0	0.578	2.4	0.632	2.0	0.649	1.88	0.655	1.84	0.5	3.0
0.9	0.645	1.9	0.697	1.55	0.709	1.47	0.714	1.44	0.605	2.2
0.6	0.829	0.8	0.858	0.7	0.865	0.65	0.865	0.65	0.785	1.05

Table 2.5.2

FILTER TYPE*	BF3	BF4	BF5	BF6	CCT
$D_{opt} = \frac{D}{G}\Big\|_{G=1} = \frac{2\Delta f_d}{B_3}$	0.902	0.828	0.806	0.804	1.0

Table 2.5.3

* BFk denotes Bessel band-pass filter of order k.
CCT denotes critically-coupled tuned filter.

Tables 2.5.1/2/3 refer to the case $\omega_c/B_{3\omega} = 30$.

To find the optimum value of G, curves of the type given in fig.2.5.1 are replotted as in fig. 2.5.2, so giving γ_r as a function of G for several values of $F(\gamma_r, G)$. The optimum value of $G(G_{opt})$ is considered to be the one which defines the minimum value of γ_r over the largest range of $F(\gamma_r, G)$. From fig. 2.5.2, it can be seen that, for the filters considered, $G_{opt} = 1$. The corresponding optimum values of D (D_{opt} say) are then given by $D/G\big|_{G=1}$ and are listed in table 2.5.3. It is interesting to note here, however, that a variation of $\pm$ 5 per cent in D about D_{opt}, which causes a $\pm$ 5 per cent variation in G about G_{opt}, will only reduce the performance of the system by about 0.1dB in γ_r. [Fig. 2.5.2 refers.]

It has been shown that in the case of G = 1 there is a closed-form solution[29] for $F(\gamma_d, G)$, viz.

$$F(\gamma_d, 1) = \tfrac{1}{2}\exp(-\gamma_d) \qquad \text{.....(2.5.11).}$$

Accordingly, the minimum error probability in discriminator detection (for the filters considered) is given by

$$P_e = \tfrac{1}{2}\exp(-a_c \gamma_r) \qquad \text{.....(2.5.12),}$$

where $$a_c \equiv \gamma_d/\gamma_r\big|_{G=1} \qquad \text{.....(2.5.13),}$$

and from the values of $\gamma_d/\gamma_r\big|_{G=1}$ (listed in table 2.5.2) a_c is seen to be filter-dependent. For the range of Bessel filters considered, however, there is (as is to be expected) a definite converging effect in the value of a_c as the filter order increases.

By/

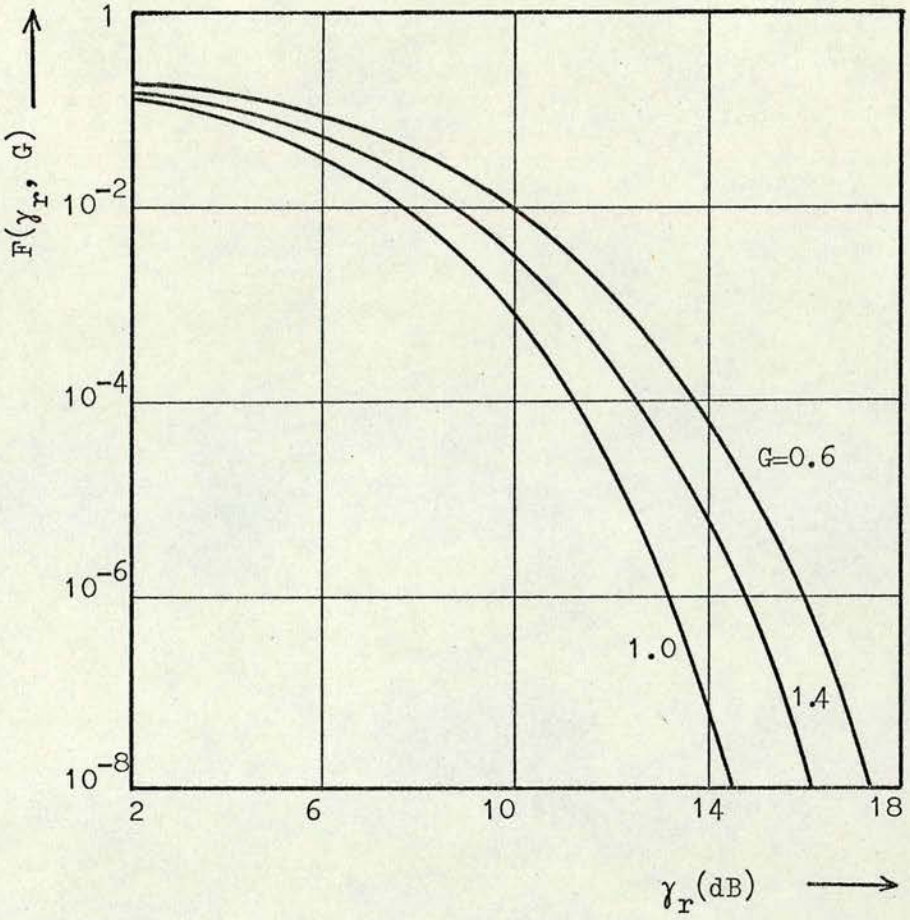


Fig. 2.5.1 Computed curves of $F(\gamma_r, G)$ for a fourth-order Bessel band-pass filter.

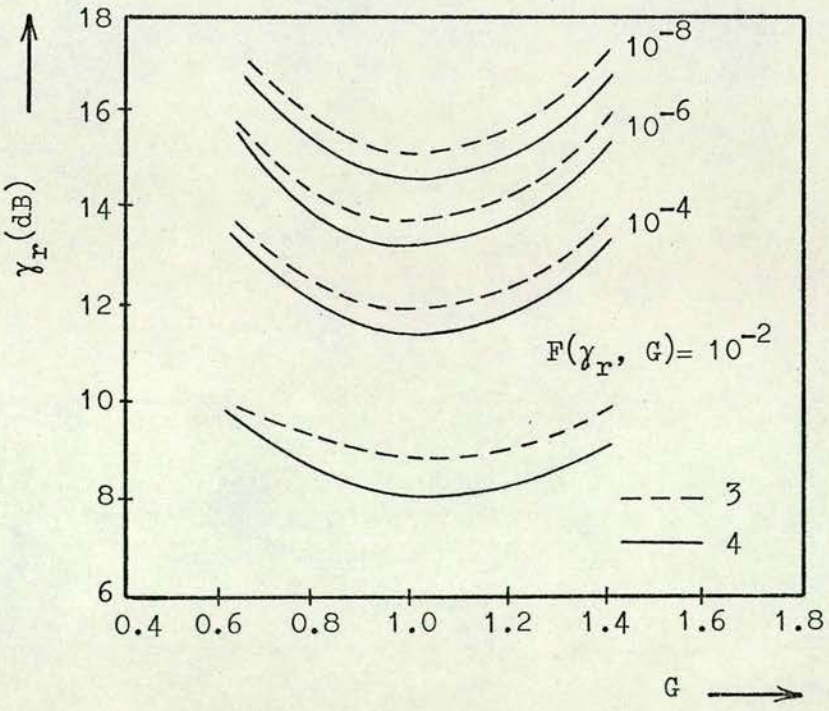


Fig. 2.5.2 Curves of γ_r vs. G with $F(\gamma_r, G)$ constant for third- and fourth-order Bessel filters.

By comparing eqns. (1.4.4) and (2.5.12), it can be seen that the minimum error probability for both 'dual-filter' envelope detection and discriminator detection (for the filters considered) have the same decaying exponential form, viz.

$$P_e = \tfrac{1}{2}\exp(-e_a \gamma_r) \qquad \text{.....(2.5.14),}$$

where for 'dual-filter' envelope detection and discriminator detection respectively,

$$e_a \equiv 0{\cdot}5 \text{ , and } e_a \equiv a_c \qquad \text{.....(2.5.15),}$$

Now γ_r, the received signal-to-noise ratio, is given by[21]

$$\gamma_r = S_r/NB \qquad \text{.....(2.5.16),}$$

where S_r is the received signal power, N is the received Gaussian noise power density, and B is the receiver band-pass filter noise-equivalent bandwidth which is defined, for <u>both</u> detection techniques, to allow the filter deterministic transient response function to reach a steady-state level in one bit period (T say). For any given filter, the parameter described (in sect. 2.4) as the filter 'bandwidth/pulse-settling-time product' (m_c say) relates the filter bandwidth requirements to the desired pulse-settling-time T by

$$B \times T = m_c \qquad \text{.....(2.5.17),}$$

and γ_r may then be rewritten as

$$\gamma_r = S_r T/Nm_c \qquad \text{.....(2.5.18).}$$

The/

The error probability given by eqn (2.5.14) then becomes

$$P_e = \tfrac{1}{2}\exp(-e_c S_r T/N) \qquad \text{.....(2.5.19),}$$

where $$e_c \equiv e_a/m_c \qquad \text{.....(2.5.20)}$$

and is filter-dependent accordingly.

Since S_r, N and T may be assumed to be the same for comparable detection systems, the error-probability performance of 'dual-filter' envelope detection and discriminator detection of binary FSK can be compared, at least for the range of filters given in (i) and (ii) above, by evaluating the parameter e_c for each system thus defined. In view of (2.5.20), however, the value of the parameter m_c must be found firstly for each of the detection filter systems to be considered.

2.6 The reponse of band-pass filters to a binary-FSK input signal

If the band-pass filter input $v_i(t)$ and output $v_o(t)$ have Laplace transforms $V_i(s)$ and $V_o(s)$ respectively, then the filter transfer function $H_b(s)$ relates $V_i(s)$ and $V_o(s)$ through[46, 47, 50, 51]

$$V_o(s) = V_i(s)H_b(s) \qquad \text{.....(2.6.1),}$$

and $$v_o(t) \equiv \mathcal{L}^{-1}\{V_o(s)\} \qquad \text{.....(2.6.2),}$$

where $\mathcal{L}^{-1}\{X(s)\}$ denotes the usual one-sided inverse Laplace transform of X(s). Of specific interest here are the transient responses of

a/

a range of band-pass filters [defined by (i) and (ii) in sect. 2.5 above] for a continuous-wave binary FSK input signal.

Simulation of such a filter input signal is achieved simply by allowing a continuous change from one frequency either ω_1 or ω_2 (as the case may be) to the other at some time (t_c say) which has allowed the previous transient response to settle. The filter input signal $v_i(t)$ can therefore be represented analytically in the form

$$v_i(t) = u(t)\cos \omega_1 t + u(t - t_c)\left[\cos\left\{\omega_2(t - t_c) + \omega_1 t_c\right\} - \cos\left\{\omega_1(t - t_c) + \omega_1 t_c\right\}\right] \qquad \text{.....(2.6.3)}$$

$$= u(t)\cos \omega_1 t + u(t - t_c)\left[\cos \omega_1 t_c \left\{\cos \omega_2(t - t_c) - \cos \omega_1(t - t_c)\right\} - \sin \omega_1 t_c \left\{\sin \omega_2(t - t_c) - \sin \omega_1(t - t_c)\right\}\right] \qquad \text{.....(2.6.4),}$$

where $u(t)$ is the Heaviside unit-step function and is defined here by

$$u(t) \equiv 1 \quad (t \geqslant 0) \quad , \quad u(t) \equiv 0 \quad (t < 0) \qquad \text{.....(2.6.5).}$$

The Laplace transform $V_i(s)$ of $v_i(t)$ is then given by[51, 52, 53]

$$V_i(s) = \frac{s}{s^2 + \omega_1^2} + \exp(-st_c)\left\{\cos \omega_1 t_c \left(\frac{s}{s^2 + \omega_2^2} - \frac{s}{s^2 + \omega_1^2}\right) - \sin \omega_1 t_c \left(\frac{\omega_2}{s^2 + \omega_2^2} - \frac{\omega_1}{s^2 + \omega_1^2}\right)\right\} \qquad \text{.....(2.6.6).}$$

From eqn. (2.6.6) the denominator roots of $V_i(s)$ are seen to be distinct/

distinct complex-conjugate pairs

$$s = \pm j\omega_x \qquad (x = 1, 2) \qquad \text{.....(2.6.7).}$$

In view of this, and since the denominator roots of $H_b(s)$ for the filters of interest also occur in distinct complex-conjugate pairs (cf. sect. 2.4 and 2.5 above), it follows that the denominator roots of $V_o(s)$ $\left[= V_i(s)H_b(s)\right]$ are distinct complex-conjugate pairs. Now a function F(s) of the form

$$F(s) \equiv N(s)/D(s) = N(s)/D_1(s)\,(s - \alpha - j\beta)(s - \alpha + j\beta) \text{.....(2.6.8),}$$

where N(s) and D(s) are real coefficient polynomials in s, with $s = \alpha \pm j\beta$ as distinct roots of D(s) such that

$$D(s) \equiv D_1(s)\,(s - \alpha - j\beta)(s - \alpha + j\beta) \qquad \text{.....(2.6.9),}$$

reduces, after partial-fraction analysis, to

$$F(s) = \frac{K_1}{s - \alpha - j\beta} + \frac{K_2}{s - \alpha + j\beta} + \frac{N_1(s)}{D_1(s)} \qquad \text{.....(2.6.10),}$$

in which $N_1(s)/D_1(s)$ is the remainder,

$$K_1 \equiv N(\alpha + j\beta)/2j\beta D_1(\alpha + j\beta) \qquad \text{.....(2.6.11),}$$

and $$K_2 \equiv N(\alpha - j\beta)/-2j\beta D_1(\alpha - j\beta) \qquad \text{.....(2.6.12).}$$

It can be shown that the constants K_1 and K_2 associated with conjugate roots are themselves conjugate so that, writing

K_1/

$$K_1 = a + jb = \tfrac{1}{2}M\exp(j\theta) \qquad \text{.....(2.6.13),}$$

where $\tfrac{1}{2}M \equiv \sqrt{(a^2 + b^2)}$ and $\tan\theta \equiv b/a$ .....(2.6.14),

we have $K_2 = a - jb = \tfrac{1}{2}M\exp(-j\theta) = K_1^*$ .....(2.6.15).

The inverse Laplace transform $f_1(t)$ of the complex-conjugate terms in eqn. (2.6.10) is then given by[51, 52, 53]

$$f_1(t) = \mathcal{L}^{-1}\left(\frac{K_1}{s - \alpha - j\beta} + \frac{K_1^*}{s - \alpha + j\beta}\right) \qquad \text{.....(2.6.16),}$$

$$= \exp(\alpha t)\left\{K_1\exp(j\beta t) + K_1^*\exp(-j\beta t)\right\} \qquad \text{.....(2.6.17),}$$

so that, on substituting for K_1 and K_1^* according to eqns. (2.6.13) and (2.6.15), we obtain

$$f_1(t) = \tfrac{1}{2}M\exp(\alpha t)\left[\exp\left\{j(\beta t + \theta)\right\} + \exp\left\{-j(\beta t + \theta)\right\}\right] \qquad \text{.....(2.6.18)}$$

$$= M\exp(\alpha t)\cos(\beta t + \theta) \qquad \text{.....(2.6.19).}$$

Similarily, by applying this general technique to $V_i(s)H_b(s)$, we obtain

$$\begin{aligned} v_o(t) = \sum_{i=1}^{k+1}\Big(& u(t)A_{i1}\exp(\alpha_{i1}t)\cos(\beta_{i1}t + \theta_{i1}) \\ & + u(t - t_c)\cos\omega_1 t_c\left[A_{i2}\exp\left\{\alpha_{i2}(t - t_c)\right\}\cos\left\{\beta_{i2}(t - t_c) + \theta_{i2}\right\}\right. \\ & \left. - A_{i1}\exp\left\{\alpha_{i1}(t - t_c)\right\}\cos\left\{\beta_{i1}(t - t_c) + \theta_{i1}\right\}\right] \\ & - u(t - t_c)\sin\omega_1 t_c\left[B_{i2}\exp\left\{\alpha_{i2}(t - t_c)\right\}\cos\left\{\beta_{i2}(t - t_c) + \psi_{i2}\right\}\right. \\ & \left.\left. - B_{i1}\exp\left\{\alpha_{i1}(t - t_c)\right\}\cos\left\{\beta_{i1}(t - t_c) + \psi_{i1}\right\}\right]\Big) \end{aligned} \qquad \text{.....(2.6.20),}$$

where the response terms associated with the cosine and sine-wave input signals [defined in eqn. (2.6.4)] have constant amplitudes A_{ix} and B_{ix}, and constant phase displacements θ_{ix} and ψ_{ix} respectively; the subscript x(= 1, 2) denotes terms associated with cosine and sine-wave input frequency ω_1 or ω_2; the subscript i is a dummy variable to facilitate a summation to (k + 1); k represents the band-pass filter order (cf. sect. 2.4 above) and the summation to (k + 1) results from the combined effect of $V_i(s)H_b(s)$ producing a denominator polynomial of order 2(k + 1). Since the complex-conjugate roots of $V_i(s)$ defined in (2.6.6) are included in the 2(k + 1) roots, it is worth noting, therefore, that one of the i subscripts (say j) defines the following,

$$\beta_{j1} \equiv \omega_1, \quad \beta_{j2} \equiv \omega_2, \qquad \alpha_{j1} \equiv \alpha_{j2} = 0,$$
$$A_{j1} \equiv B_{j1}, \quad A_{j2} \equiv B_{j2}, \quad \theta_{j1} = \psi_{j1} + \pi/2, \quad \theta_{j2} = \psi_{j2} + \pi/2$$

.....(2.6.21).

For the practical filters of interest here, $\alpha_{ix}(i \neq j\ ;\ x = 1,2)$ is negative so that $\exp(\alpha_{ix}t) \to 0$ as $t \to \infty$. Accordingly, for $t \gg t_c$, eqn. (2.6.20) reduces to

$$v_o(t) = A_{j1}\cos(\beta_{j1}t + \theta_{j1})$$
$$+ \cos\omega_1 t_c \left[A_{j2}\cos\left\{\beta_{j2}(t - t_c) + \theta_{j2}\right\} - A_{j1}\cos\left\{\beta_{j1}(t - t_c) + \theta_{j1}\right\}\right]$$
$$- \sin\omega_1 t_c \left[B_{j2}\cos\left\{\beta_{j2}(t - t_c) + \psi_{j2}\right\} - B_{j1}\cos\left\{\beta_{j1}(t - t_c) + \psi_{j1}\right\}\right]$$

.....(2.6.22).

By/

By applying the results of (2.6.21) to eqn. (2.6.22), it follows that

$$v_o(t) = A_{j1}\cos\left\{\omega_2(t - t_c) + \theta_{j2} + \omega_1 t_c\right\} \quad (t \gg t_c) \quad \ldots\ldots(2.6.23),$$

which is the residual filter output signal after all the transient effects have settled; i.e. A_{j1} represents the steady-state level of the envelope response, and $(\theta_{j2} + \omega_1 t_c)$ represents the steady-state level of the excess-phase response taken with respect to a frequency ω_2.

Since the time of switching t_c is variable, the excess-phase reference level in eqn. (2.6.23) is deemed to be θ_{j2}. The transient effects in the excess-phase response after the switching time t_c are therefore derived with respect to θ_{j2}, this being achieved by adding and subtracting $\left\{\omega_2(t - t_c) + \theta_{j2}\right\}$ to the phase angle of each cosine term in eqn. (2.6.20). These cosine terms have the general form $g_c(t')$ given by

$$g_c(t') = \cos(\beta_{ix}t' + \lambda_{ix}) \quad \ldots\ldots(2.6.24),$$

where t' is either t or $(t - t_c)$, and λ_{ix} is either θ_{ix} or ψ_{ix}. After adding and subtracting the phase term $\left\{\omega_2(t - t_c) + \theta_{j2}\right\}$, $g_c(t')$ becomes

$$g_c(t') = \cos\left\{\beta_{ix}t' - \omega_2(t - t_c) + \lambda_{ix} - \theta_{j2}\right\}\cos\left\{\omega_2(t - t_c) + \theta_{j2}\right\}$$

$$- \sin\left\{\beta_{ix}t' - \omega_2(t - t_c) + \lambda_{ix} - \theta_{j2}\right\}\sin\left\{\omega_2(t - t_c) + \theta_{j2}\right\}$$

$\ldots\ldots(2.6.25)$.

Resubstituting/

Resubstituting for $g_c(t')$[as given by eqn. (2.6.25)]in eqn. (2.6.20) and collecting like terms, we find that $v_o(t)$ may be represented by

$$v_o(t) = r_{oc}(t)\cos\left\{\omega_2(t - t_c) + \theta_{j2}\right\} - r_{os}(t)\sin\left\{\omega_2(t - t_c) + \theta_{j2}\right\} \quad \ldots\ldots(2.6.26),$$

where

$$\begin{matrix} r_{oc}(t) \\ r_{os}(t) \end{matrix} \equiv \sum_{i=1}^{k+1} \left(u(t)A_{i1}\exp(\alpha_{i1}t)\begin{matrix}\cos \\ \sin\end{matrix}\left\{\beta_{i1}t + \theta_{i1} - \omega_2(t - t_c) - \theta_{j2}\right\}\right.$$

$$+ u(t - t_c)\cos\omega_1 t_c \left[A_{i2}\exp\left\{\alpha_{i2}(t - t_c)\right\}\begin{matrix}\cos \\ \sin\end{matrix}\left\{(\beta_{i2} - \omega_2)(t - t_c) + \theta_{i2} - \theta_{j2}\right\}\right.$$

$$\left. - A_{i1}\exp\left\{\alpha_{i1}(t - t_c)\right\}\begin{matrix}\cos \\ \sin\end{matrix}\left\{(\beta_{i1} - \omega_2)(t - t_c) + \theta_{i1} - \theta_{j2}\right\}\right]$$

$$- u(t - t_c)\sin\omega_1 t_c \left[B_{i2}\exp\left\{\alpha_{i2}(t - t_c)\right\}\begin{matrix}\cos \\ \sin\end{matrix}\left\{(\beta_{i2} - \omega_2)(t - t_c) + \psi_{i2} - \theta_{j2}\right\}\right.$$

$$\left.\left. - B_{i1}\exp\left\{\alpha_{i1}(t - t_c)\right\}\begin{matrix}\cos \\ \sin\end{matrix}\left\{(\beta_{i1} - \omega_2)(t - t_c) + \psi_{i1} - \theta_{j2}\right\}\right]\right) \quad \ldots\ldots(2.6.27).$$

The envelope response $e_o(t)$, excess-phase response $\phi_o(t)$ and time derivative of the excess-phase response $\dot{\phi}_o(t)$ (which is of particular interest in discriminator detection) are then found by further simplifying eqn. (2.6.26) to

$$v_o(t) = e_o(t)\cos\left\{\omega_2(t - t_1) + \theta_{j2} + \phi_o(t)\right\} \quad \ldots\ldots(2.6.28),$$

where

$$e_o(t) \equiv \sqrt{\left\{r_{oc}^2(t) + r_{os}^2(t)\right\}} \quad \ldots\ldots(2.6.29),$$

and/

and $$\phi_o(t) = \tan^{-1}\left\{r_{os}(t)/r_{oc}(t)\right\} \qquad \text{.....(2.6.30),}$$

$\dot{\phi}_o(t)$ then being given by

$$\dot{\phi}_o(t) = \frac{r_{oc}(t)\dot{r}_{os}(t) - r_{os}(t)\dot{r}_{oc}(t)}{r_{os}^2(t) + r_{oc}^2(t)} \qquad \text{.....(2.6.31).}$$

From the form of $r_{oc}(t)$ and $r_{os}(t)$ given in (2.6.27), it is obvious that the final expressions for $e_o(t)$, $\phi_o(t)$ and $\dot{\phi}_o(t)$ become extremely complicated; they are not therefore reproduced here.

A digital computer program (described in appendix 2) was developed to carry out the tedious mathematical computations required to evaluate to $e_o(t)$, $\phi_o(t)$ and $\dot{\phi}_o(t)$ as functions of time for the band-pass filter systems of interest. The filter responses investigated may be classified as those obtained for a continuous-wave binary FSK input to

(i) a discriminator detection filter system with the keying-frequency separation optimised [according to $D_{opt}(=2\Delta f_d/B_3)$, as listed in table 2.5.3] for the filters being considered, and

(ii) a 'dual-filter' envelope detection filter system with the keying-frequency separation chosen, for the same range of filters as in (i), to give an approximately 20dB difference between the 'in-band' and 'out-of-band' signal power levels. [It is tentatively assumed that this condition gives a good approximation to the ideal 'dual-filter' envelope detection system (discussed in sect. 2.2).]

Let/

Let us consider firstly the filter responses for the discriminator detection systems defined by (i) above. According to the discussion of sect. 2.3, $e_o(t)$ and $\dot{\phi}_o(t)$ are of particular interest in this detection technique. These responses are illustrated in fig. 2.6.1 for two of the filter systems being considered, viz

(a) a fourth-order Bessel band-pass filter (denoted by BF4), and

(b) a critically-coupled tuned band-pass filter (denoted by CCT),

both filters having $B_3 = 1\text{Hz}$ and $f_c = 30\text{Hz}$ (thus satisfying the filter symmetry requirements of sect. 2.4). In both cases, the input signals are switched continuously from a low to a high frequency at a time t_c (which has allowed all previous transient effects to setle), the signal frequency separation being chosen according to (i) above.

From the curves of fig. 2.6.1, it can be seen that a turning point due to some overshoot (which is virtually indistinguishable from the steady-state level) occurs in the corresponding $e_o(t)$ and $\dot{\phi}_o(t)$ responses at the same measured time (say t_d) after time t_c. Since this feature is found for all the filter systems considered, the time periods $t_d - t_c$ measured for each filter are therefore deemed to be the transient settling times for those filter responses. The 'bandwidth/pulse-settling-time product' m_c is then found for these discriminator detection filter systems as

$$m_c = B(t_d - t_c) \qquad \text{.....(2.6.32).}$$

Substituting/

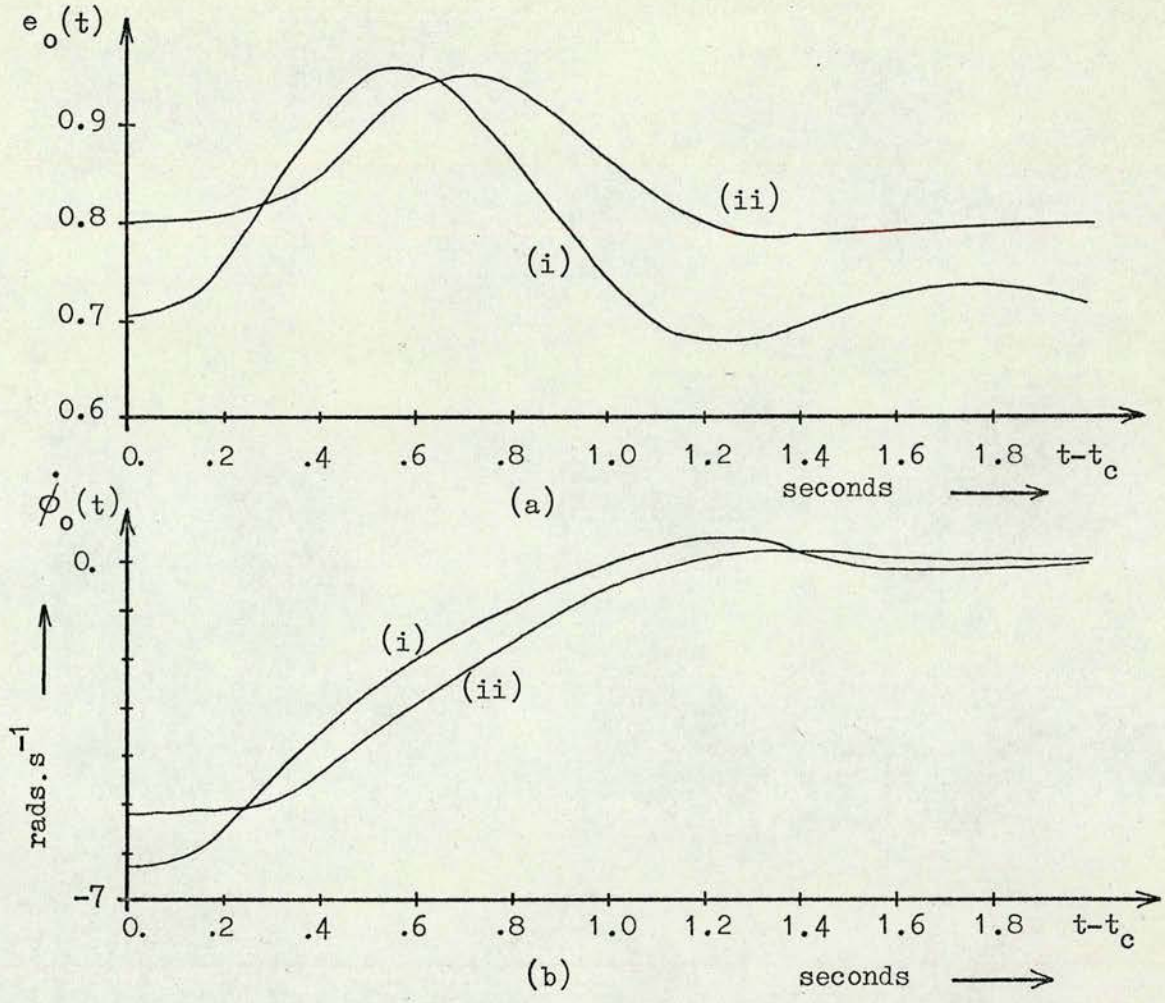


Fig. 2.6.1 The responses (a) $e_o(t)$, and (b) $\dot{\phi}_o(t)$ for optimum discriminator detection incorporating the filter types* (i) CCT, and (ii) BF4 with $B_3 = 1$Hz.

FILTER TYPE*	$\frac{\omega_2-\omega_1}{B_{3\omega}}$	m_{c3}		
		$\omega_1 \rightarrow \omega_2$	$\omega_2 \rightarrow \omega_1$	max.
BF3	0.902	1.31	1.32	1.32
BF4	0.828	1.37	1.37	1.37
BF5	0.806	1.45	1.44	1.45
BF6	0.804	1.53	1.52	1.53
CCT	1.0	1.25	1.25	1.25

Table 2.6.1

*BFk denotes Bessel band-pass filter of order k

CCT denotes critically-coupled tuned filter

Substituting for B according to (2.5.10) results in

$$m_c = c_1 B_3(t_d - t_c) = c_1 m_{c3} \quad \text{.....(2.6.33),}$$

where $$m_{c3} \equiv B_3(t_d - t_c) \quad \text{.....(2.6.34).}$$

Since the filter transfer functions are defined with respect to their 3dB bandwidths B_3, it is more convenient at this point, therefore, to evaluate m_{c3}.

The values of m_{c3} found for the discriminator detection filter systems considered are listed in table 2.6.1. Since the filters are asymmetrical (although only slightly so) m_{c3} is evaluated for both frequency steps ω_1 to ω_2 and ω_2 to ω_1. The maximum value of m_{c3} obtained for each filter may then be used to describe its comparative quality as a discriminator detection filter system.

Now let us consider the filter responses for the 'dual-filter' envelope detection systems defined by (ii) above. According to the discussion of sect. 2.2, $e_o(t)$ and $\phi_o(t)$ are of particular interest in this detection technique. These responses are illustrated in fig. 2.6.2 for the same filter types considered in fig. 2.6.1.

From the curves of fig. 2.6.2, it can be seen that a turning point due to some overshoot (which, again, is virtually indistinguishable from the steady-state level) occurs in the $e_o(t)$ response at a time t_e (say) after

t_c/

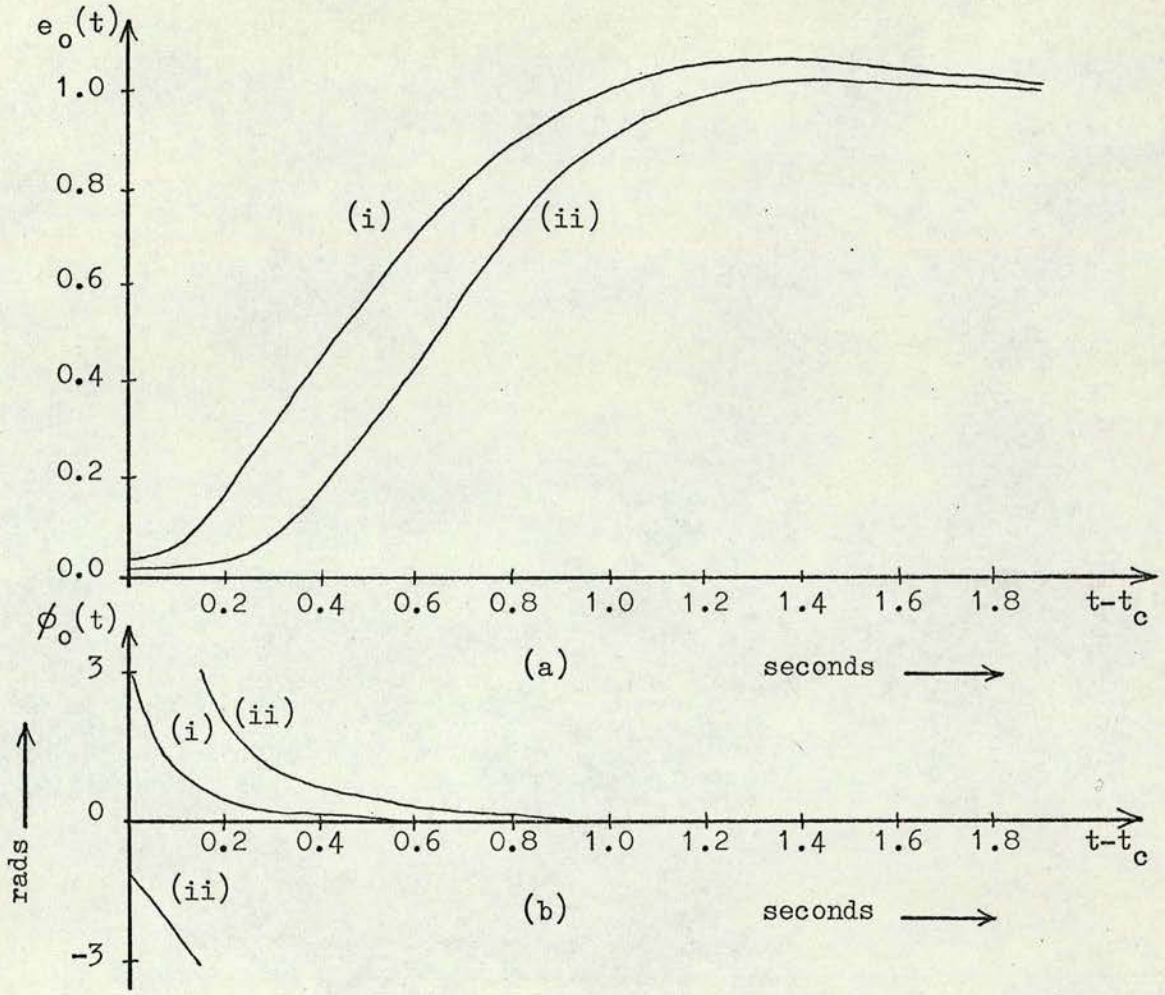


Fig. 2.6.2 The responses (a) $e_o(t)$, and (b) $\phi_o(t)$ for 'dual-filter' envelope detection incorporating the filter types* (i) CCT, and (ii) BF4 with B_3 = 1Hz.

FILTER TYPE*	$\frac{\omega_2-\omega_1}{B_{3\omega}}$	m_{c3}		
		$\omega_1 \rightarrow \omega_2$	$\omega_2 \rightarrow \omega_1$	max.
BF3	2.6	1.46	1.29	1.46
BF4	2.0	1.48	1.32	1.48
BF5	1.8	1.52	1.36	1.52
BF6	1.6	1.56	1.40	1.56
CCT	3.0	1.41	1.12	1.41

Table 2.6.2

*BFk denotes Bessel band-pass filter of order k
CCT denotes critically-coupled tuned filter

t_c, whilst the $\phi_o(t)$ response is seen simply to decay to a steady-state level (viz. zero in the cases considered). It is found, for the filter systems considered, that the time required for $\phi_o(t)$ to decay to within $\pi/100$ rads of the steady-state phase angle is less than the time period $t_e - t_c$. The time period $t_e - t_c$ is therefore deemed to be the transient settling time and m_{c3} for these 'dual-filter' envelope detection systems is then given by

$$m_{c3} = B_3(t_e - t_c) \qquad \text{.....(2.6.35).}$$

The values of m_{c3} found for the 'dual-filter' envelope detection systems considered are listed in table 2.6.2. As with the discriminator detection systems examined, m_{c3} is evaluated for both frequency steps ω_1 to ω_2 and ω_2 to ω_1. The maximum value of m_{c3} obtained for each filter may then be used to describe its comparative quality as a 'dual-filter' envelope detection system.

The values of m_{c3} thus derived (and listed in tables 2.6.1 and 2.6.2) together with the minimum error probability characteristics derived in previous sections, now facilitate a theoretical comparison of the performance of 'dual-filter' envelope detection and discriminator detection of continuous-wave binary FSK.

2.7 The choice of detection technique (discriminator detection)

It was shown in sect. 2.5 that the minimum error-probability characteristics for/

for 'dual-filter' envelope detection and discriminator detection of binary FSK have the same decaying exponential form [viz. $P_e = \frac{1}{2}\exp(-e_c S_r T/N)$] and may be compared by evaluating the parameter e_c for both techniques. It follows from (2.6.33) and (2.5.20) that e_c may be given by

$$e_c = e_a/c_1 m_{c3} \qquad \ldots\ldots(2.7.1),$$

where the parameters e_a, c_1 and m_{c3} have been derived above for a range of filters applicable to both detection techniques. In particular, for the discriminator detection systems, the values of m_{c3} and e_a $(=\gamma_d/\gamma_r\big|_{G=1})$ are listed in tables 2.6.1 and 2.6.2 respectively, whilst for the 'dual-filter' envelope detection systems, $e_a \equiv 0{\cdot}5$ [cf. (2.5.15) above] and the values of m_{c3} are listed in table 2.6.2. The values of c_1 (applicable to both types of system) are listed in table 2.5.1.

Accordingly, e_c may now be evaluated and the resulting values are listed in table 2.7.1 for both detection techniques. Some of the corresponding error-probability characteristics are also shown plotted in fig. 2.7.1. Two observations can be made from these results, viz.

(i) that the error-reduction properties of the discriminator detection systems are better than those of the 'dual-filter' envelope detection systems [the worst P_e characteristic obtained for discriminator detection with a critically-coupled tuned filter (denoted by CCT) being better than the best P_e characteristic obtained for envelope detection with a fourth-order Bessel filter (denoted by BF4)], and

(ii) that,/

FILTER TYPE*	$e_c = e_a/c_1 m_{c3}$	
	DISC. DET.	ENV. DET.
BF3	.407	.318
BF4	.440	.322
BF5	.430	.316
BF6	.412	.308
CCT	.360	.319

Table 2.7.1

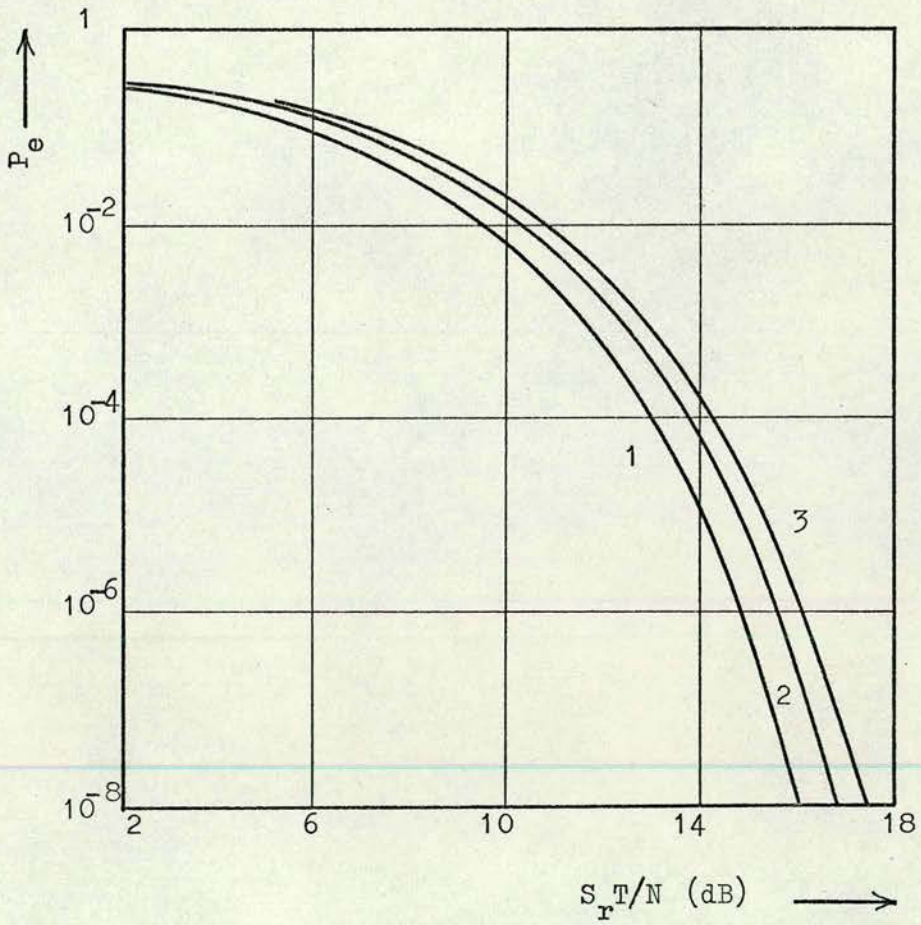


Fig. 2.7.1 Probability of error P_e as a function of S_rT/N for*

(1) discriminator detection incorporating filter BF4,

(2) discriminator detection incorporating filter CCT, and

(3) 'dual-filter' envelope detection incorporating filter BF4.

*BFk denotes Bessel band-pass filter or order k

CCT denotes critically-coupled tuned filter

(ii) that, of the filters considered, the fourth-order Bessel filter is the best approximation to a 'matched' filter for both detection techniques (the best error-probability characteristic being provided by this filter in both cases).

Observation (i) provides the theoretical justification for choosing discriminator detection as the receiver detection technique for the telemetry system being investigated. However, since the error-probability characteristic derived for discriminator detection holds only for $\gamma_r > 4$dB (cf. sect. 2.3 above), we must investigate the practical significance of this limit before making a final choice of detection technique.

From eqns. (2.5.14) to (2.5.20) it follows that

$$S_r T/N = e_a \gamma_r / e_c \qquad \ldots\ldots(2.7.2),$$

and a value of $S_r T/N$ corresponding to $\gamma_r = 4$dB may therefore be defined for each of the detection systems considered here. In particular, for the best discriminator detection and 'dual-filter' envelope detection systems [defined in (ii) above], the corresponding values of $S_r T/N$ are 5·6dB and 5·9dB respectively. From fig. 2.7.1, it can be seen that these values give $P_e \approx 0{\cdot}1$ for both systems. Since accurate data retrieval is impossible by either detection technique at this level of error-probability, γ_r will be required to be greater than 4dB for useful operation. The results of table 2.7.1 and the observations of (i) and (ii) will therefore hold for practical systems. Accordingly, discriminator detection is chosen as the receiver detection technique in this telemetry system.

This/

This completes the definition of the proposed digital telemetry system. The remainder of this thesis is concerned with the design and experimental assessment of a prototype system.

CHAPTER 3

THE TRANSMITTER SYSTEM DESIGN

3.1 General

According to the brief specification of the proposed prototype transmitter source given in sect. 1.5, the digital telemetry system to be investigated can be described as a 5-data-channel PCM/continuous-wave FSK system.

In the PCM part of the transmitter source, the five data channels are sampled sequentially (at a minimum frequency of 1KHz), each sample then being quantised to within the desired resolution (one per cent of the signal dynamic range), and the resulting quantised levels binary encoded for serial transmission. A 7-bit binary code allows 128 ($= 2^7$) possible combinations (normally referred to as data/code words) giving a possible resolution of 1/128 of the dynamic range.

Corresponding to the signal levels set aside for synchronisation purposes in TDM/PAM systems (cf. sect. 1.2 above), however, some code combinations are set aside for synchronisation purposes in TDM/PCM systems. Specifically, code combinations are normally set aside for a frame synchronisation word (FS word) and possibly also for a sub-frame synchronisation word (SFS word) if subcommutation is employed (which is not the case for this prototype system). One frame of information in this prototype TDM/PCM system therefore comprises five data words and an FS word.

In many cases the signal statistics of the biological information to be transmitted will be unknown, with the result that the frequency distributions of each data word (and therefore of each binary digit) will also be unknown. What must be postulated, therefore, is that the average rate of occurence of each binary digit will vary continuously as a function of the data. Accordingly, if the PCM waveform modulates the transmitter oscillator directly (bearing in mind the effects of capacitive coupling discussed in sect. 1.4), the average rate of occurrence of the two FSK frequencies will be data-dependent. This feature will impair the performance of the possible receiver FSK detection techniques (considered in chapter 2 above) since automatic frequency control (AFC), which operates on information concerning <u>average</u> frequency, is required in the receiver system (cf. sect. 4.2 below).

The problem is overcome, however, by arranging that the 7-bit data words are, in turn, encoded into data words having equal numbers of the two distinct binary symbols present. (Such coding will be described as <u>balanced</u>.) The average value of the balanced-code waveform is constant, which results in the average value of the transmitter keying frequencies being constant (except possibly for oscillator drift effects). Accordingly, the performance of the receiver detection technique is not impaired, since the receiver AFC combats the effects of frequency drifts.

In many systems, an extra encoding process is included at the output of the PCM encoder to allow the receiver system to detect (and possibly to correct) errors in the regenerated bit pattern[54].

It should be noted that although an extra encoding process is included in this system (as described above), no specific attempt is made to implement an error detection/correction code as such. The reason for this is that in most biological research applications the redundancy in the transmitted data allows data-compression techniques to be used, thereby averaging out the effects of small error rates on the detected data words.

A block diagram of the prototype digital transmitter system is given in fig. 3.1.1. The function and design of each block is considered in the following sections of this chapter.

3.2 The balanced encoder

A 7-bit binary code has 128 possible data words. Specifically, the problem is to relate these data words directly with a set of balanced-code words which have an equal number of each binary digit present.

In this application, the minimum number of bits required per balanced-code word is found as the smallest even integer satisfying the inequality

$$\frac{x!}{(x/2)!^2} \geqslant 128 \qquad \text{.....(3.2.1).}$$

For x=8 there are 70 possible balanced code words, and for x=10 there are 252 such. Accordingly, the minimal number of bits required is ten.

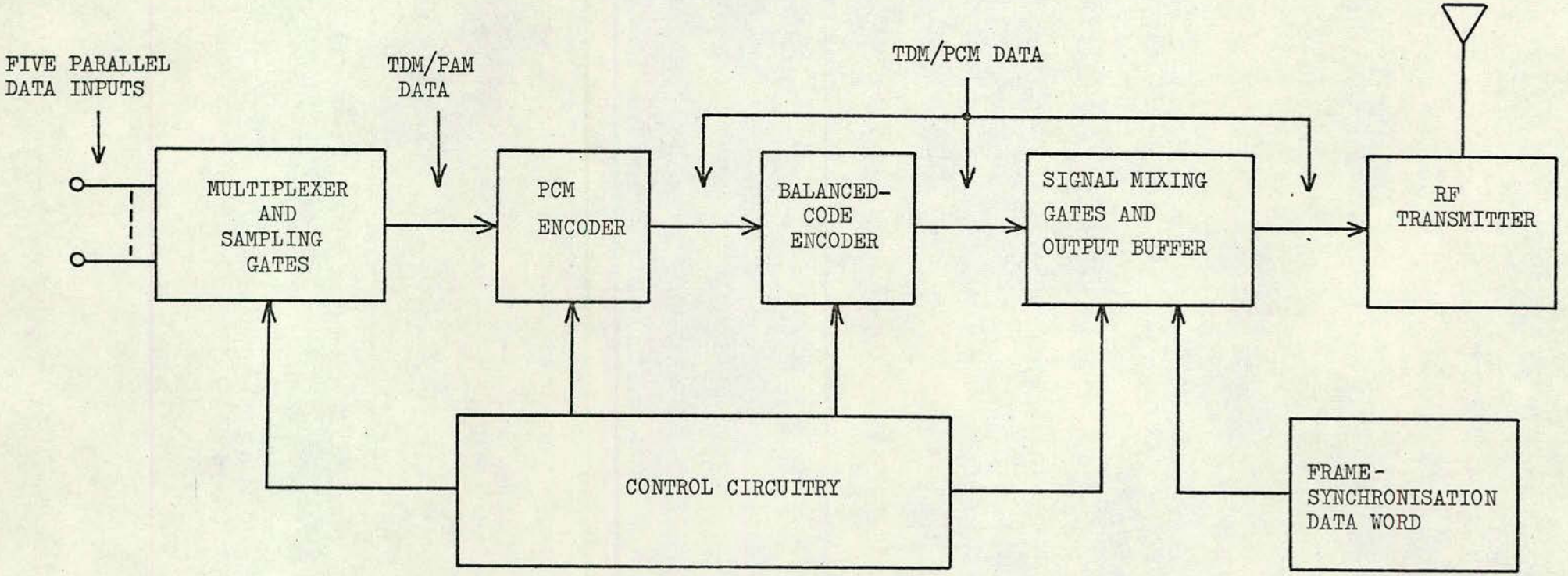


Fig. 3.1.1 Block diagram of the prototype digital transmitter system.

The implementation of an encoding process for this 10-bit code was investigated and found to be quite complex. An estimation of the required number of COS/MOS medium-scale-integration devices is similar to that required for the rest of the PCM system. At this level of complexity the implementation of this particular encoder becomes too expensive for further consideration either in the prototype system built with discrete MSI devices or in a final special-purpose microcircuit package suitable for implantation.

The easiest code to implement is a 14-bit code generated from the 7-bit binary code and its complement, which is obtained through simple logic inversion. Such a code is obviously obtained at the expense of a greater transmitted bit rate. However, since the minimisation of transmission bandwidth is not paramount, whilst the basic simplicity of the transmitter source is still a consideration, it was decided to implement a 14-bit balanced code in the present system. In particular, if a 7-bit binary code is represented as 'B1, B2 ... B7' (say), then the corresponding 14-bit balanced code is represented as 'B1, $\overline{B1}$, B2 ... $\overline{B6}$, B7, $\overline{B7}$'. This code structure is chosen since it provides a rapidly changing serial data stream which is a useful feature for receiver bit-synchronisation purposes (cf. sect. 4.3 below).

By way of compensating for the greater transmission bandwidth, the 14-bit balanced code has two other features which can be used to advantage in the telemetry receiver system:-

(i) Such a 14-bit code provides 3432 ($= 14!/7!^2$) balanced-code words with which to encode the 128 data words of the 7-bit binary code. The redundancy in coding facilitates the implementation of a basically simple frame-synchronisation process through the selection of an FS word which is significantly different from all other possible data patterns (cf. sect. 4.4 below). If b_c represents the number of bit coincidences between a trial code word and any other pattern of 14-bits, then the cross-correlation coefficient r_c between the two 14-bit patterns is defined by

$$r_c \equiv b_c - (14 - b_c) = 2b_c - 14 \qquad .....(3.2.2).$$

The code word '11110110010000' was found to have the best cross-correlation coefficient pattern (given in fig. 3.2.1), the number of bit coincidences between this code word and any other possible bit pattern for transmission being at most ten. This code word was chosen as the FS word for the present system accordingly.

(ii) Since the 14-bit code is generated from a combination of a 7-bit binary code and its complement, an error (or rather the possibility of an error) is detectable in any bit position of the final received 7-bit code by simply testing for complementation in the correct bit positions of the received 14-bit code. The use of this error-detecting facility depends to a great extent on the further processing of the received data, but in general it provides a facility for rejecting badly corrupted data.

[1	1	1	1	0	1	1	0	0	1	0	0	0	0]	b_c	r_c
0	1	0	1	0	1	1	0	0	1	0	1	0	1	10	6
1	1	0	1	0	1	0	1	0	1	0	1	0	[1	9	4
0	1	0	1	0	1	1	0	0	1	1	0	[1	1	9	4
1	1	0	1	0	1	0	1	0	1	0	[1	1	1	8	2
0	1	0	1	0	1	1	0	0	1	[1	1	1	1	8	2
1	1	0	1	0	1	0	0	1	[1	1	1	1	0	8	2
0	1	0	1	0	1	1	0	[1	1	1	1	0	1	8	2
1	1	0	1	0	1	0	[1	1	1	1	0	1	1	7	0
0	1	0	1	0	1	[1	1	1	1	0	1	1	0	8	2
1	1	0	1	0	[1	1	1	1	0	1	1	0	0	8	2
0	1	0	1	[1	1	1	1	0	1	1	0	0	1	8	2
1	0	1	[1	1	1	1	0	1	1	0	0	1	0	10	6
0	1	[1	1	1	1	0	1	1	0	0	1	0	0	7	0
1	[1	1	1	1	0	1	1	0	0	1	0	0	0	9	4
[1	1	1	1	0	1	1	0	0	1	0	0	0	0]	14	14
1	1	1	0	1	1	0	0	1	0	0	0	0]	0	9	4
1	1	0	1	1	0	0	1	0	0	0	0]	0	1	7	0
1	0	1	1	0	0	1	0	0	0	0]	0	1	0	10	6
0	1	1	0	0	1	0	0	0	0]	0	1	0	1	8	2
1	1	0	0	1	0	0	0	0]	1	0	1	0	0	8	2
1	0	0	1	0	0	0	0]	0	1	0	1	0	1	8	2
0	0	1	0	0	0	0]	1	0	1	0	1	0	0	7	0
0	1	0	0	0	0]	1	0	0	1	0	1	0	1	8	2
1	0	0	0	0]	0	1	1	0	1	0	1	0	0	8	2
0	0	0	0]	0	1	1	0	0	1	0	1	0	1	8	2
0	0	0]	1	0	1	0	1	0	1	0	1	0	0	8	2
0	0]	1	0	0	1	1	0	0	1	0	1	0	1	9	4
0]	1	0	1	0	1	0	1	0	1	0	1	0	0	9	4
1	0	1	0	0	1	1	0	0	1	0	1	0	1	10	6

Fig. 3.2.1 The pattern of bit-coincidence coefficients b_c and cross-correlation coefficients $r_c (= 2b_c - 14)$ of the FS word [11110110010000] with the worst-possible combinations of data bits.

In the present system, the desired 14-bit code can be obtained as a parallel output from the PCM encoder (cf. sect. 3.4 below).

3.3 The PCM encoder

The process of PCM encoding is also referred to as A/D (analogue-to-digital) conversion. It is the process of generating the series of n bits (7 in this case) which quantise the value of an analogue signal sample to a desired resolution. Of the various techniques available for A/D conversion [55,56,57], the successive approximation method was chosen since it was found to require the simplest analogue circuitry for implementation in the present system (cf. subsection 3.3.3 below).

In principle, the successive approximation A/D convertor operates by making a feedback voltage V_{da} approximate an input voltage V_{sh} in a sequence of successive steps. For the first step, V_{da} is made equal to $V_r/2$, where V_r is some constant reference voltage. For each subsequent step, however, V_{da} is changed in accordance with the result of a comparison between V_{sh} and the previous value of V_{da}. The amount by which V_{da} is increased or decreased is $V_r/2^x$, where x defines the x-th step in the operation. Only one step per binary-code bit is therefore required for any conversion.

A circuit/block diagram of the prototype A/D conversion system is given in fig. 3.3.1. The operation of this system is most simply described by firstly considering the operation of its two major logic elements, viz. the 7-bit ring counter (referred to here as BRC), and the 7-bit store (referred to here as FF).

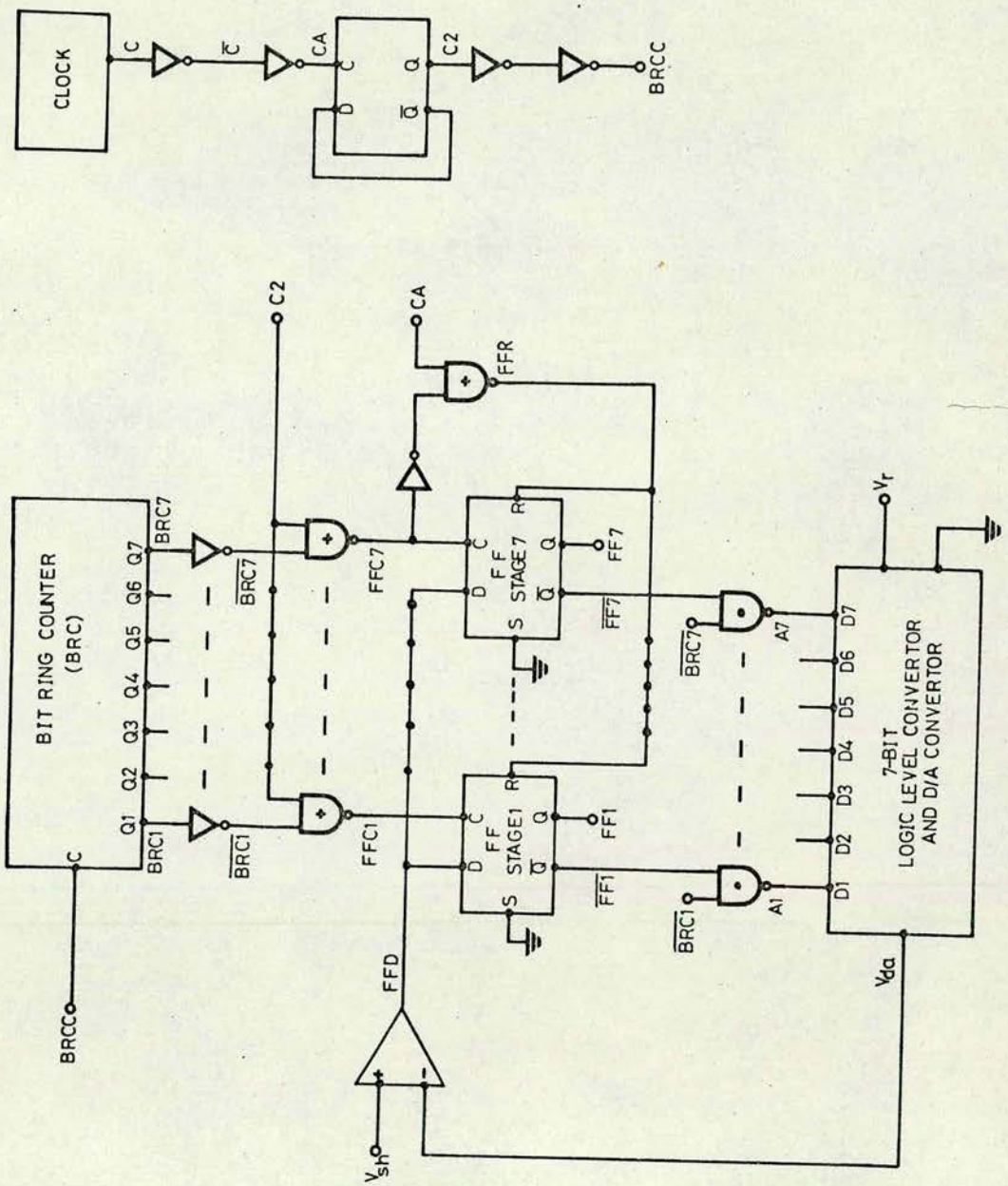


Fig. 3.3.1 A circuit/block diagram of the A/D conversion system.

The ring counter BRC is of standard form. (The design is considered later in subsection 3.3.2.) It is defined here, however, as having a single circulating bit. Specifically, a single '1' bit exists in the ring and appears at each output (denoted here by BRCx, for x = 1 to 7) in turn, the moves from stage to stage being made synchronously with the positive-pulse-edge transitions of a clock-input function (denoted here by BRCC).

The store FF comprises seven parallel D-type flip-flops with a common data input (denoted here by FFD) and a common reset function (denoted here by FFR). Each flip-flop, however, has a separate clock-input function (denoted here by FFCx, for x=1 to 7). Data held on FFD are stored separately at each FF output (denoted here by FFx, for x = 1 to 7) synchronously with the positive-pulse-edge transitions of the corresponding clock-input functions.

The input voltage V_{sh} is obtained by a sample-and-hold device (described later in sect. 3.4) whilst the feedback voltage V_{da} is obtained at the output of a D/A convertor. A binary code, representing the value of V_{da} derived after each trial voltage step in the approximation process, is stored in the parallel outputs of FF. With the outputs of FF being reset to '0' for the start of each quantisation process, the successive trial voltage levels are obtained on the D/A conversion of a binary code generated by the addition of the parallel outputs from FF and BRC. Here, binary addition is equivalent to a simple OR function of the BRC and FF outputs. For fabrication with COS/MOS, however, a NAND function is more useful, so that in terms of bit position x the adder output Ax becomes

$$Ax = \overline{\overline{BRCx} \cdot \overline{FFCx}} \quad (x = 1 \text{ to } 7) \qquad \ldots\ldots(3.3.1).$$

(The bar is used to denote the inverse logic function here.) Each trial voltage obtained by the D/A conversion of the adder binary output code is compared with V_{sh}. If the trial voltage is smaller than V_{sh}, the comparator output has the value '1' which is then stored in the FF position corresponding to the approximation step number. On the other hand, if the trial voltage is greater than V_{sh}, the comparator output has the value '0'. The storage of this bit value has no significance since each FF position is initially reset to '0'.

Consider now the operation of this A/D conversion process for an input voltage level $V_{sh} = \frac{3}{4} V_r + \delta$ (say), where $\delta < V_r/128$. Initially, the FF outputs are reset to '0', and BRC output position one contains the circulating bit. These FF and BRC codes have the equivalent D/A conversion voltage levels of 0 and $V_r/2$ respectively, so that their summation gives a first-trial voltage level of $V_r/2$. Now $V_{sh} > V_r/2$, producing the comparator output '1' which is then stored in position FF1. For step two, the FF and BRC output codes have the equivalent D/A conversion voltage levels of $V_r/2$ and $V_r/4$ respectively, so that their summation gives a second-trial voltage level value $3\ V_r/4$. Now $V_{sh} > 3V_r/4$, producing the comparator output '1' which is then stored in position FF2. For step three, the FF and BRC output codes have the equivalent D/A conversion voltage levels of $3\ V_r/4$ and $V_r/8$ respectively, so that their summation produces a third-trial voltage level of value $7V_r/8$. Now $V_{sh} < 7V_r/8$, producing the comparator output '0' which is already stored in position FF3. This process continues through the required seven steps to generate the FF output code '1100000' which is the desired A/D conversion output for an input signal of value $3V_r/4 + \delta$.

The operation of the process thus described is dependent upon the generation of the relevant control functions for BRC and FF [as discussed respectively in (i) and (ii) above]. A timing diagram showing these control functions in relation to other system logic functions (shown in fig. 3.3.1) is given in fig. 3.3.2. This timing diagram should therefore be used for reference purposes in the following discussion of these system logic control functions.

From the example above, it is obvious that the seven steps of successive approximation are generated by clocking round the BRC stages. The pulse frequency of the clock-input function BRCC is therefore determined by the desired transmission rate for a 7-bit binary code. In this system, however, the clock generator (cf. subsection 3.3.1 below) output function C has a pulse frequency corresponding to the transmission rate for the chosen 14-bit balanced-code (cf. sect. 3.2 above). Consequently, the control function BRCC is obtained from the system clock function through the binary module shown in fig. 3.3.1. Two invertor stages are used before and after the binary stage to spread the capacitive loading on the various control functions.

In view of a system design feature (to be discussed in some detail later in sect. 3.4) half the BRC clock-input period is allowed for the processes of addition, D/A conversion, and comparison. Accordingly, the comparator output is clocked into FF synchronously with the negative-pulse-edge transition of BRCC associated with the bit position being investigated. For COS/MOS implementation, therefore, the store clock input to stage x is given by

$$\overline{FFCx} = \overline{C2 + \overline{BRCx}} \qquad (x = 1 \text{ to } 7) \qquad \ldots\ldots(3.3.2),$$

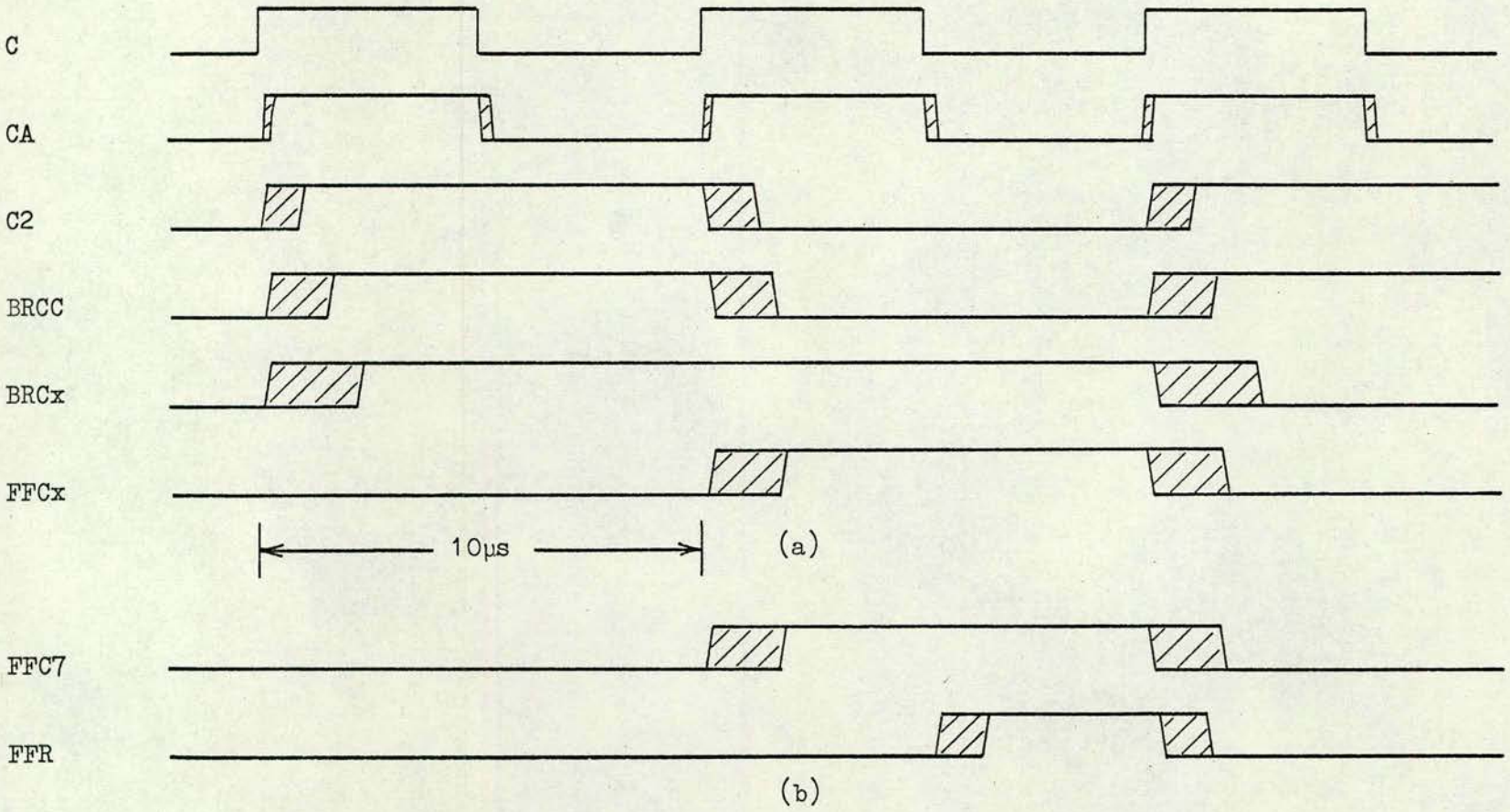


Fig. 3.3.2 Timing diagram showing the expected variations (hatched)
(a) between the general A/D convertor control waveforms, and
(b) between the store reset waveform FFR and the store clock input FFC7.

where C2 (as shown in fig. 3.3.1) is isolated from BRCC by two invertor stages.

On receipt of the positive-pulse-edge transition of FFC7, the A/D conversion of a particular sample is completed and held in the output stages of the store FF. Accordingly, there are three other control operations associated with the FFC7 pulse, viz.

(i) the parallel outputs of FF are clocked synchronously with the positive-pulse-edge transition of $\overline{C}$ into an output buffer register for serial transmission (cf. sect. 3.5 below);

(ii) the FF outputs are reset to '0' before the start of the next sample approximation process, so that with the synchronous data transfer described in (i), the reset function FFR can be defined by the same pulse, specifically

$$FFR = \overline{\overline{FFC7} + CA} \qquad \text{.....(3.3.3),}$$

where CA is isolated from C by two invertor stages; and

(iii) the encoded signal sample is replaced by the next sample for encoding (cf. sect. 3.4 below).

Some other design aspects are also worthy of consideration, viz.

(a) the clock generator design,

(b) the ring counter design,

(c) the D/A convertor design, and

(d) the comparator design.

These items are considered in turn.

3.3.1 The clock circuit

The circuit diagram of the clock generator is given in fig. 3.3.3 from which it can be seen to comprise an astable multivibrator circuit with a divide-by-two output stage. This type of multivibrator circuit has three basic operational features, viz.

(i) that the frequency variation is less than one per cent for a one volt change in power-supply voltage,

(ii) that the frequency stability is virtually independent of temperature (there being very little change in device parameters with temperature), and

(iii) that the duty cycle of the output waveform is in general not 50 per cent and, moreover, it is not easily controlled.

Since the clock output is used in a variety of system applications, it is desirable that the duty cycle should be easily reproduced. This is easily achieved by allowing the multivibrator to run at twice the desired frequency and then dividing by two (using the D-type flip-flop as shown) to produce the desired frequency with a fixed 50 per-cent duty cycle.

Since the largest clock frequency in this system is required for the serial transmission of the final 14-bit balanced-code words (cf. sect. 3.5 below), it is therefore specified by the corresponding frequency f_b(say) of the transmitted balanced-code bits. In particular, if n_b is the number of bits per balanced-code word, n_c is the number of channels per transmitted frame, and f_s is the channel sampling frequency, then f_b is simply given by [10,11,12]

$$f_b = n_b n_c f_s \qquad \text{.....(3.3.4).}$$

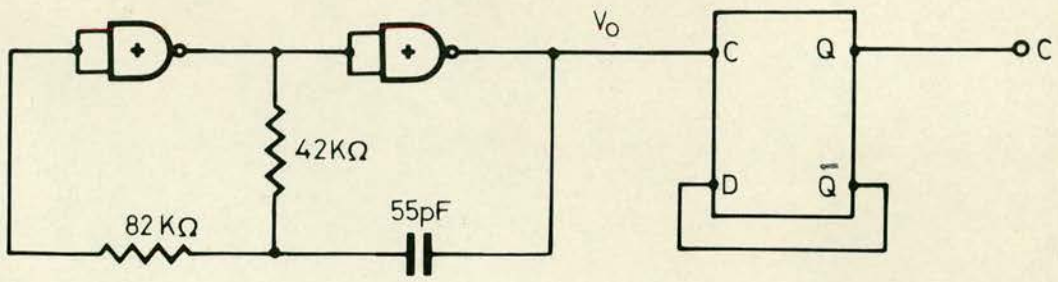


FIG. 3.3.3 Circuit diagram of the 100KHz clock generator.

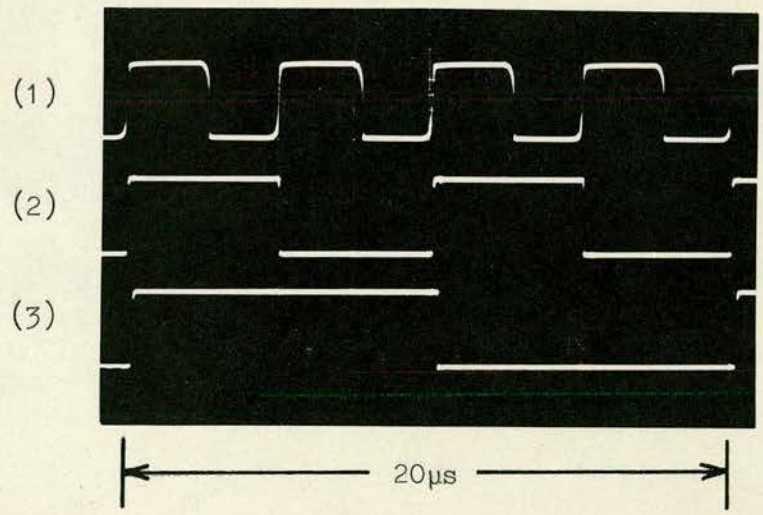


FIG. 3.3.4 Oscilloscope traces showing the relationship between

(1) the multivibrator output signal,

(2) the generated clock function C, and

(3) the ring counter clock input function BRCC.

To satisfy the transmission requirements of the prototype system, then, f_b is required to be at least 84 KHz. For test purposes, f_b is set at 100 KHz accordingly. The oscilloscope traces of fig. 3.3.4 illustrate the resulting divide-by-two relationship between the multivibrator output signal, the generated clock waveform, and the ring counter clock-input signal BRCC.

This clock circuit is suitable for implantation. In particular, the two timing resistors will be conveniently produced on a thin-film substrate whilst the capacitor will be bonded to the substrate at no great loss in thin-film area (n.b. very small chip capacitors[58] are now available for this purpose).

3.3.2 The ring counter design

In an application of this type it is particularly important that some form of self-correcting ring counter should be used. The circuit diagram of the standard self-correcting ring counter used here is shown in fig. 3.3.5. In general, n-1 shift register outputs are decoded to correct an n-bit ring counter. If DS is the shift register serial-data input and Qx (x = 1 to 7) defines the shift register output terminals, then decoding is achieved in this case simply by

$$DS = \overline{Q1 + Q2 + Q3 + Q4 + Q5 + Q6} \qquad .....(3.3.5),$$

although the combination of NAND and NOR gates (shown in fig. 3.3.5) is necessary for implementation with the existing COS/MOS devices.

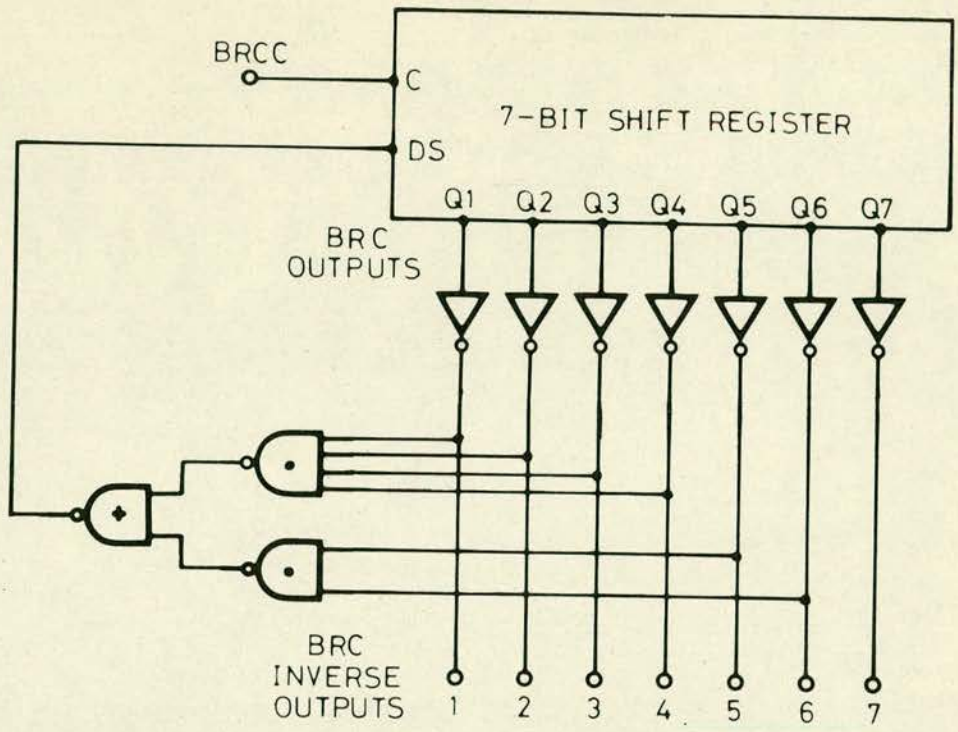


FIG. 3.3.5 Circuit diagram of ring counter BRC.

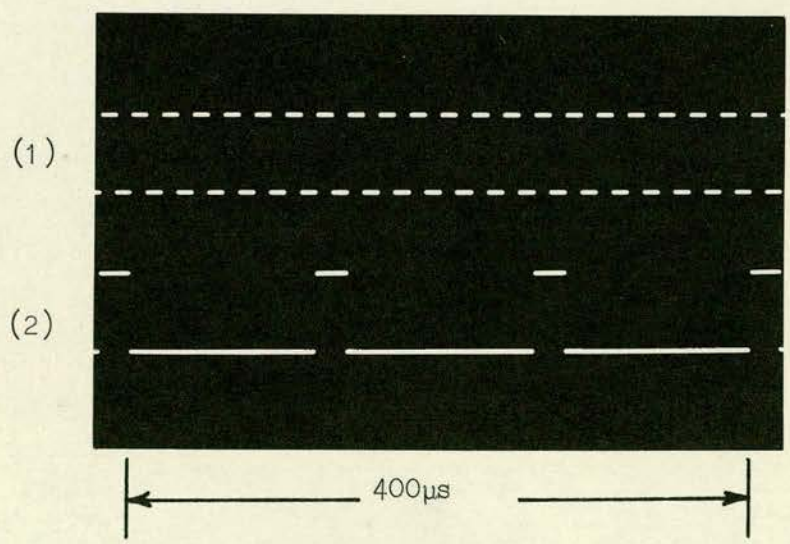


FIG. 3.3.6 Oscilloscope traces showing the divide-by-seven relationship between

(1) the ring counter clock input function BRCC, and

(2) the shift register data input function DS.

A further advantage of this type of ring counter is that it requires no special starting circuitry, provided (as in this application) that time is available for the ring counter to correct the circulating bit pattern. The ring counter requires at most one complete cycle, or seven clock pulses, to insure that the correct bit pattern is circulating. This self-correcting process occurs in a post-switch-on transient period which is not usually monitored at the receiver.

The oscilloscope traces of fig. 3.3.6 show the divide-by-seven relationship obtained in practice between BRCC and DS.

3.3.3 The D/A convertor circuit

The D/A conversion circuit converts a binary coded number into an analogue voltage which is directly proportional to the number to be decoded. Normally the binary code is arranged on parallel lines to control the switching of either a reference voltage or current source into a resistance network which produces the desired numerical solution. As shown in fig. 3.3.7, this system uses the controlled switching of a reference voltage source into a resistance (R-2R) ladder circuit. If V_{da} is the analogue representation of the binary code, then it can be shown, (by successive use of Thévenin's theorem) that [55,56,57]

$$V_{da} = \sum_{x} V_x/2^x \qquad \ldots\ldots(3.3.6),$$

where V_x has the value either V_r or 0 volts (as the case may be) in the ideal case.

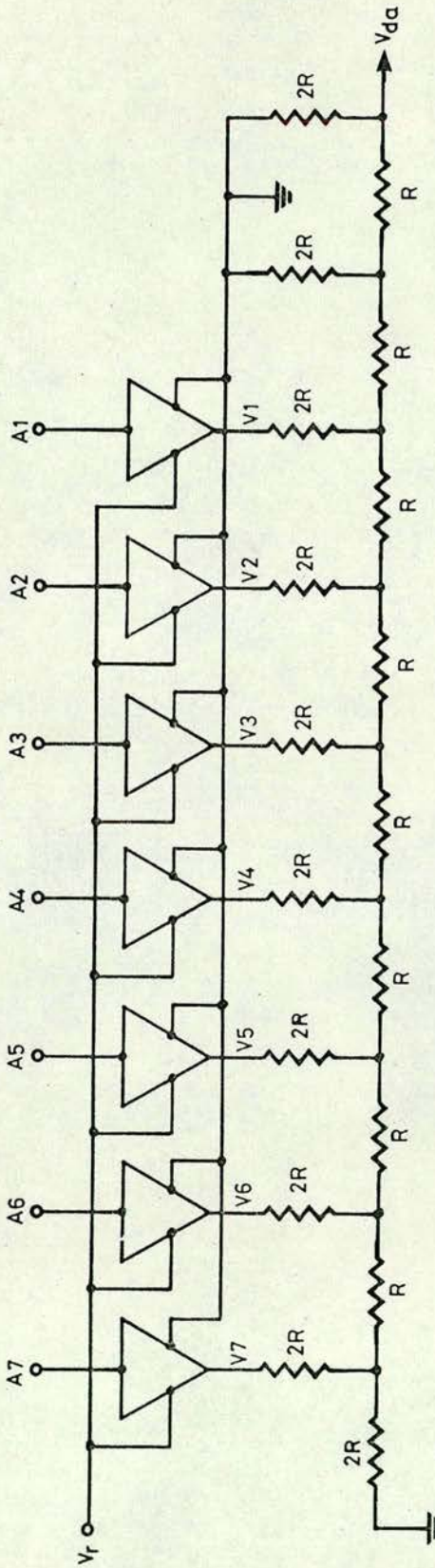


Fig. 3.3.7 The D/A convertor circuit.

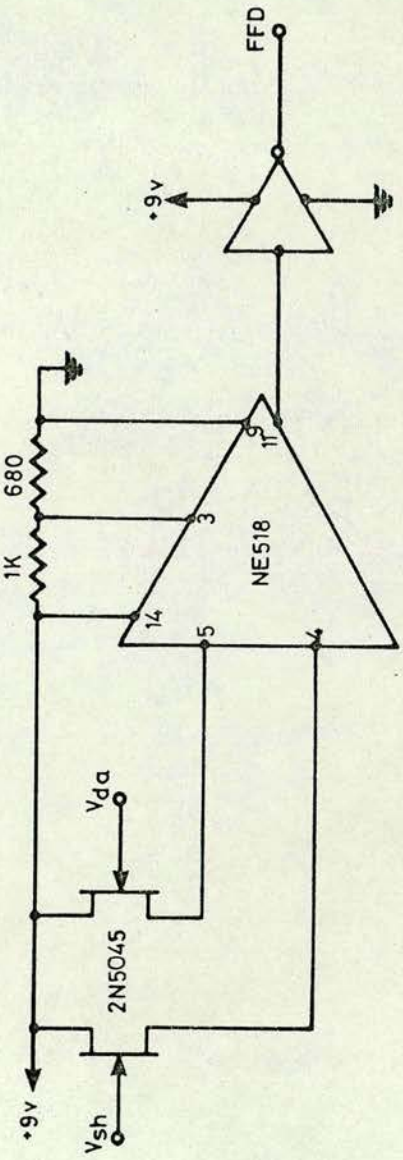


Fig. 3.3.8 The comparator circuit.

There are normally three main problems associated with the D/A conversion process:-

(i) Variations in temperature cause variations in the values of R and 2R in the resistance ladder. However, this will not be a major problem in an implanted environment (which can be considered to have a constant temperature). In fact, temperature effects can be neglected even in the trial system which uses a thick-film R-2R ladder that has a maximum output voltage error [59] of $\pm$ 0.0122 per cent over the temperature range $-55^{o}C$ to $125^{o}C$. This voltage error is about 100 times smaller than the desired signal resolution of one per cent.

(ii) The output resistance R_o of the voltage source causes an error in the D/A conversion since the effective '2R' value becomes $2R + R_o$. In many cases this output resistance can be specified accurately so that the value of 2R can be reduced by R_o to compensate for the additive effect. This method of compensation is not possible in the system considered here in which the COS/MOS buffer amplifiers (providing the most suitable interfacing circuitry) have an output resistance that varies with logic level. To compensate in this case, the value of R is increased so that the value of 2R is much larger than the maximum value of R_o.

Changes in the value of 2R effectively result in a variation of the quantisation step level. This type of error has been analysed[55] by supposing that in addition to the normal quantising noise there is also an additive noise due to the variations in quantising step level.

For small variations[55] (within 5 per cent of the quantising step level), however, the resulting noise is negligible in comparison to the normal quantising noise. For the present system, an 'R' value of 50 KΩ (so that[8] $R_o/2R < 0.1$) has been shown[60] by computer simulation to give variations in quantisation step level of less than 5 per cent. This value of R was therefore chosen to define the ladder network.

(iii) Variations in the value of the reference voltage V_r applied to the ladder network also cause the quantisation step level to change. It is normal practice, however, to ensure that any variations in V_r are much less than the desired signal resolution. Unfortunately, this requires extra 'analogue' circuitry which is undesirable from the point of view of implantation. An alternative is to use the normal power supply voltage as V_r and, by monitoring this (utilising one of the telemetry data channels), to provide a receiver-based reference signal with which to make any necessary compensatory adjustments. Since the extra circuitry required to monitor V_r is much less than that required to control V_r, the foregoing technique is more suitable for implantation. In the present system, the power supply voltage is used as V_r accordingly.

It should be noted here that the ladder network is essentially a voltage-level convertor so that, besides being used for D/A conversion, additional stages can be used to adjust both the D/A convertor dynamic range and offset voltage level for compatibility with the comparator circuit. For this prototype system, two extra stages are added thereby attenuating the dynamic range to $V_r/4$ and giving zero D/A conversion offset voltage.

In most A/D conversion systems, the output of the ladder network current drives some buffer amplifier which provides for faster operation by presenting a low output impedance to any capacitive load at the comparator input. However, the speed of operation is not of paramount importance here and is exchanged for simplicity in design. In particular, the D/A convertor output is connected directly to the comparator input. The output resistance of the ladder network[55,56,57] can be shown to be R so that with an expected maximum capacitive load C of 10pF in the present system, the resulting time constant RC is 500ns. Accurate D/A conversion here (i.e. to within 0.1 per cent of the convertor dynamic range) then requires 4μs(= 8RC). [A practical point to note here is that this time of 4μs is added to the time delays of the comparator and logic elements in order to obtain the minimum A/D conversion-step time (cf. subsection 3.3.4 below).]

From the practical point of view of implantation, the important considerations are the D/A convertor size and power consumption. In this prototype system, a thick-film ladder network was used since it was the cheapest available. For implantation, however, a thin-film network has a much smaller size. Preliminary calculations show that a thin-film substrate of size 1cm by 1cm (which is acceptable for implantation[25]) is more than adequate for the 50 - 100KΩ ladder network used here.

The maximum power consumption of the ladder network can be approximated by considering that the reference voltage V_r feeds eight '2R' resistors.

For a maximum power supply voltage of 9 volts and a '2R' value of 100KΩ, the current drain is 720 μA and the corresponding power consumption is ≈6.3mW. This level of power consumption is significantly larger than that required by the COS/MOS logic circuitry but is not unacceptable on comparison with the power consumption of other implanted devices[5,6,7,25]. The '50 - 100K' ladder network used here is therefore considered to be suitable for implantation as a thin-film circuit.

3.3.4 The comparator circuit

The comparator circuit designed for the prototype system is shown in fig. 3.3.8. Matched high frequency JFETS[61] were used at the comparator inputs to provide a high load impedance for a sample-and-hold circuit (which is considered in the next section). A commercially available integrated circuit comparator was used to expedite the testing of the complete system. In particular, the Signetics NE518 voltage comparator[62] device was chosen to suit a low-voltage power supply (9 volts) and thus be compatible with COS/MOS.

It should be noted here that the current drain of such commercially available comparators is considerable (20mA in this case) so that their use in implantable systems is impractical. In general, however, these high current levels facilitate extremely fast operation which is not (as was shown in the previous subsection) a major design criterion in this system. For implantation, it should therefore be possible with a discrete component design to sacrifice comparator speed for a much lower current drain.

The specification of such a low speed comparator is given here as follows:-

(i) For compatibility with a following COS/MOS input stage[8], the logic output levels should be at least 50 per cent of the supply voltage and, moreover, should be positioned symmetrically within the supply voltage range.

(ii) In view of the characteristics of the D/A convertor ladder network (cf. subsection 3.3.3 above), the input conditions may be chosen freely.

(iii) The small-signal gain is defined with respect to (i) and (ii) above; for a desired resolution of $V_r/512$ and for an output voltage swing of $V_r/2$ (as in this case) then the required gain is of the order of 300.

(iv) The current drain should be less than 500μA for practical implantation.

(v) For compatibility with the present system, the upper limit to the A/D conversion-step time upon implementing the low-speed comparator should be 10μs [i.e. half the BRC clock-input period (cf. sect. 3.4 below)].

In view of (v) above, we conclude this discussion by noting that the present system (with a high speed comparator) has an A/D conversion-step time of around 5μs, comprising 4μs for D/A conversion (cf. subsection 3.3.3 above) and an estimate of at most 1μs for accumulated time delays in the logic elements.

3.4 The multiplexer/sample-and-hold circuit

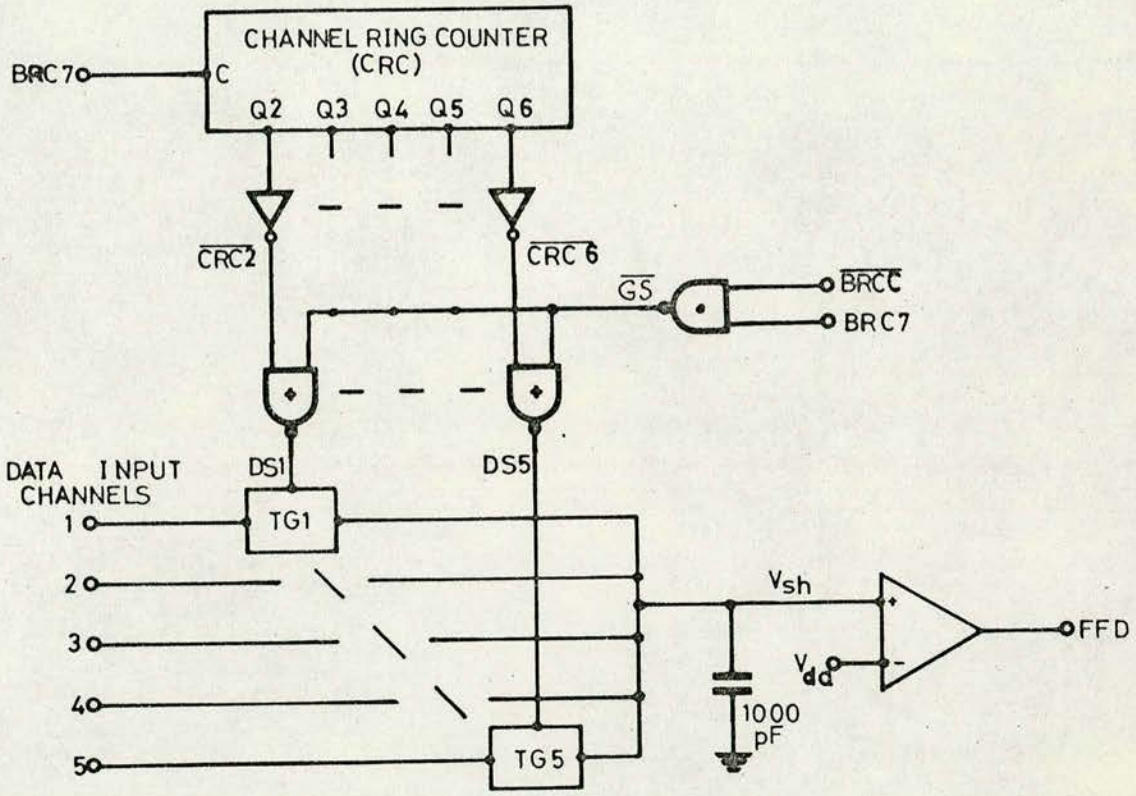
A circuit/block diagram of the multiplexer/sample-and-hold system is given in fig. 3.4.1. We consider firstly the design of the sample-and-hold process.

Sampling of the information signals is achieved by use of COS/MOS transmission gates[8]. The transmission gate acts essentially as a switch which presents a low series impedance to the sample 'holding' device when interrogated and a high series impedance when not interrogated. In this system the 'holding' device is a capacitor situated in parallel with the inverting JFET comparator input.

When a transmission gate is interrogated, the capacitor takes up the voltage appearing at the input terminal with a time constant defined by $R_{on}C_{sh}$; where C_{sh} is the capacitor value and R_{on} is the sum of the transmission gate impedance and the output impedance of a previous transducer buffer stage. One design criterion, therefore, is that the capacitor should acquire the value of the input signal to within 0.1 per cent within the period of interrogation T_i, which is the case provided that

$$7\ R_{on}\ C_{sh} \leq T_i \qquad \text{.....(3.4.1).}$$

Except for comparatively minor leakage effects, the capacitor 'holds' the value of the information signal present at the end of the interrogation period until the process of A/D conversion is completed. Leakage effects in the JFET input to the comparator predominate and can be as large[61] as 10nA. A second design criterion, therefore, is that the capacitor voltage should not change by more than 10 per cent of the quantisation step height σ in the total time required for A/D conversion, i.e./



Note

TG denotes transmission gate

Fig. 3.4.1 A circuit/block diagram of the multiplexer/sample-and-hold system.

$$\left|\frac{dV_{sh}}{dt}\right|_{max} = 10^{-8}/C_{sh} \leq \sigma f_b/140 \qquad \ldots\ldots(3.4.2),$$

where V_{sh} is the capacitor 'hold' voltage and f_b is the bit frequency.

The inequality (3.4.2) defines the acceptable minimum value of C_{sh}. Thus, for the A/D conversion system considered in sect. 3.3 above, with a minimum expected power supply voltage of 8 volts, (implying that $\sigma = 8/512$ volts) and a bit frequency of 100 KHz, the minimum value of C_{sh} is 900pF.

From the form of inequality (3.4.1), it can be seen that the allowed value of R_{on} can be maximised by minimising the value of C_{sh} and by maximising the value of T_i. The maximising of R_{on} is a particularly useful feature for implantation since it allows greater flexibility in the design of a transducer buffer stage. In view of this, the chosen value of C_{sh} is 1000pF, which is just greater than the minimum value of C_{sh} specified above. The choice of a maximum value for T_i, on the other hand, entails a system design compromise (which is explained as follows).

Referring back to the discussion in sect. 3.3, channel sampling occurs after the completion of the last step of A/D conversion and before the start of the next conversion process. Since each conversion step occurs during the corresponding BRC output pulse period, BRC7 therefore defines both the last step of A/D conversion and the channel sampling period. Accordingly, the maximum allowed value of T_i is found by subtracting the maximum time required for A/D conversion from the BRC7 output pulse period.

In the present system with a clock generator pulse frequency of 100 KHz, the BRC clock-input pulse frequency is 50 KHz and each BRC output has a pulse period of 20μs. Due to the effect of time delays (as illustrated in fig. 3.3.2), however, the effective pulse period may be reduced to 18μs. The time required for each A/D conversion step on the other hand is 5μs (cf. subsection 3.3.4 above). The maximum time allowed for channel sampling is 13μs, accordingly.

To avoid the use of extra timing circuitry, however, the channel sampling period is conveniently isolated in the BRC7 pulse period by utilising the BRC clock-input function BRCC. In particular, the channel sampling-control function GS is given by

$$GS = \overline{BRCC}.BRC7 \qquad .....(3.4.3),$$

and this restricts the sampling period to be in the second half of the BRC7 output pulse period. [Accordingly, the time allowed for each A/D conversion step is then equivalent to the first half of the corresponding BRC output pulse periods.] The allowed value of T_i here is therefore 10μs (i.e. half the BRC7 pulse period), which is just less than the maximum allowable as specified above.

On substituting [in expression (3.4.1)] the values of T_i and C_{sh} thus derived, the maximum allowed value for R_{on} becomes 1400Ω. Of this figure, 300Ω will be the maximum contribution[8] of the transmission-gate 'on' resistance. Consequently, the safe maximum allowable output impedance of a previous driving stage is 1000Ω. This is a useful impedance level allowing great flexibility in design.

The function of a driving stage is essentially to provide an interface between a biological transducer and the corresponding sampling gate. Since different driving stages are likely to be required for each tranducer, their design is best considered with respect to the individual tranducer circuits (which are not our concern in this thesis). It is sufficient here to specify

(i) that the information signals have source impedances of at most 1000Ω (as above), and

(ii) that the information signals have a dynamic range from 0 to $V_r/4$ volts for compatibility with the A/D conversion system (cf. subsection 3.3.3 above).

Having thus considered the design of the channel sample-and-hold process, we consider next the time-division-multiplexing arrangements. In this system, the TDM frame structure is defined by clocking round the stages of ring counter CRC which has a single circulating bit and is designed in the same way as BRC (cf. subsection 3.3.2 above). Specifically, the channel sampling control function GS [defined in (3.4.3) above] is applied to each data channel in turn under the control of the CRC output functions (denoted here by CRCy, y = 1 to 6). If DSy denotes the resulting sampling functions for data input channel y, then for COS/MOS implementation in this system

$$DSy = \overline{\overline{GS} + \overline{CRCy+1}} \quad (y = 1 \text{ to } 5) \qquad .....(3.4.4).$$

[The unused ring-counter output CRC1 essentially provides for frame synchronisation.]

To obtain the correct channel sampling frequency CRC may be clocked by any BRC output position. The use of BRC1, however, is to be avoided since, having regard to the channel sampling function GS [expression (3.4.3) above refers], this BRC output function causes a race condition which may produce spurious timing pulses to corrupt the sampling process. In this system, the CRC clock input control function chosen is BRC7 which is closest in phase (besides BRC1) to GS.

The process thus described facilitates the sampling of five data-input channels. It remains, however, to discuss the processing of the extra channel required for synchronisation purposes. [This is considered in the next section.]

3.5 The signal mixing gates and output buffer store

The circuit diagram of the signal mixing gates and output buffer store is given in fig. 3.5.1. The output buffer store is a 14-stage synchronous parallel-input/serial-output shift register. Parallel/serial (P/S) entry to the shift register is made synchronously with the positive-pulse-edge transitions of the clock-input function and is controlled by a P/S input selection function PSC. The mixing gates essentially block the parallel output data from the balanced encoder and present the FS word (viz. '11110110010000', as discussed in sect. 3.2 above) to the parallel inputs of the output buffer store on command.

In view of the previous discussion in sect. 3.3 and 3.4, the correct output procedure is that the synchronisation word should be clocked into the buffer shift register for output during the approximation process of the sample from the first data-input channel.

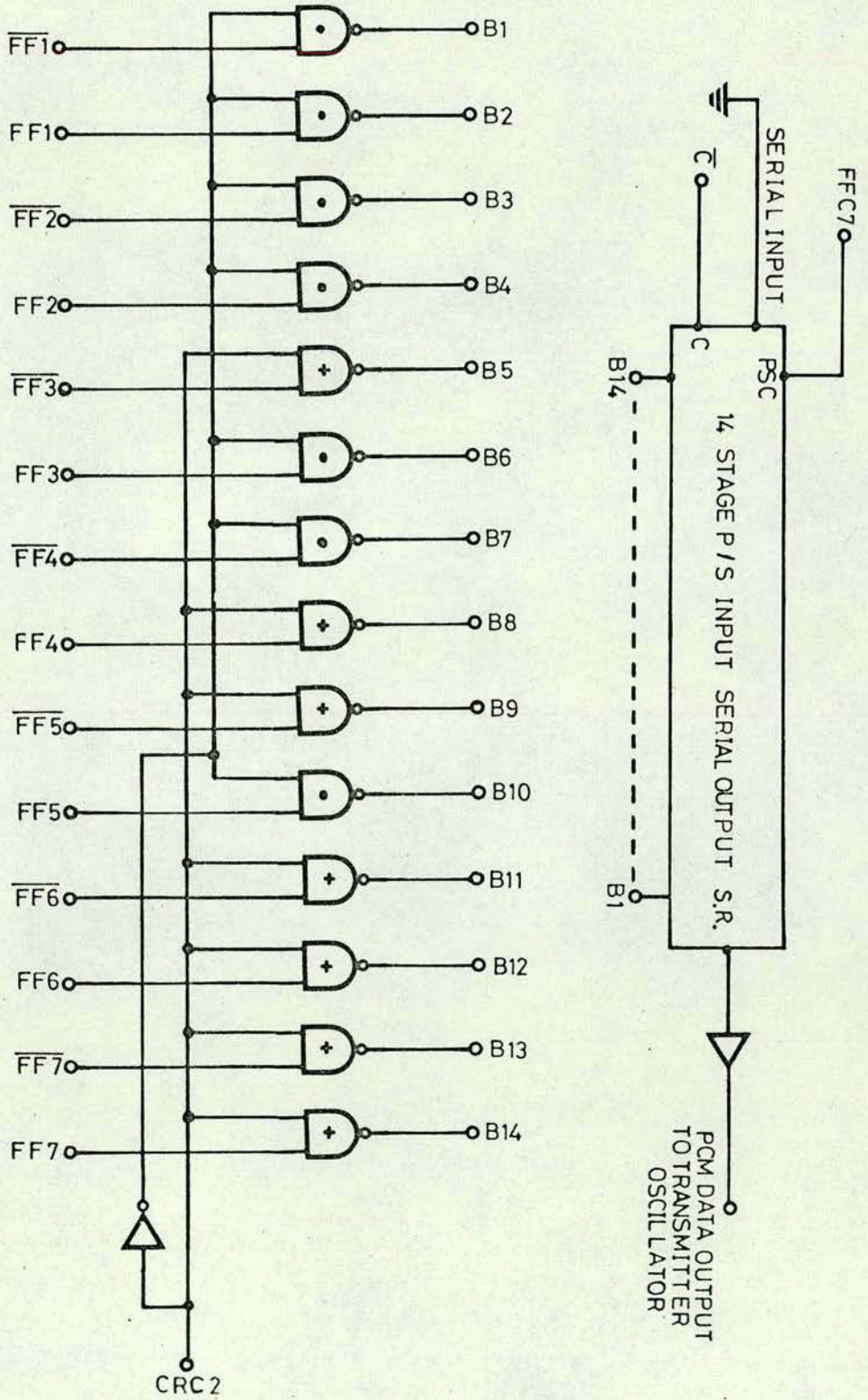


Fig. 3.5.1 Circuit diagram of the signal-mixing gates and output-buffer store.

The control function for the mixing gates is therefore conveniently chosen as the CRC2 output pulse period which also defines the sampling of the first data-input channel (cf. sect. 3.4 above). If a general parallel input to the mixing gates is denoted by GI, then, on command a NAND function produces a logic '1' at the corresponding output GD as implemented by

$$GD = \overline{GI.\overline{CRC2}} \qquad .....(3.5.1),$$

whilst a NOR function produces a logic '0' at the corresponding output GR as implemented by

$$GR = \overline{GI + CRC2} \qquad .....(3.5.2).$$

These NAND and NOR gates are arranged in sequence to produce the FS word on command. It should be noted here that the mixing gates cause an inversion such that $GO = \overline{GI}$ in both cases when the command function is not pulsed (i.e. when CRC2 is '0'). To compensate, the output from the balanced encoder should also be inverted.

In the present system, the 14-bit balanced-code words are obtained (along with the 7-bit binary code words) at the output of the A/D conversion store FF by utilising both the non-inverted and inverted store outputs. In particular, the 14-bit balanced code structure '$FF1, \overline{FF1}$, -----$FF7, \overline{FF7}$', is implemented according to the choice of code given previously. (Sect. 3.2 above refers.) It can be seen from fig. 3.5.1 that this code is suitably inverted at the input to the sampling gates.

Since the A/D conversion process is completed and the resulting codes (both binary and balanced codes) are stored in the FF outputs on receipt of the positive-pulse-edge transition of control function FFC7,/

this same function is conveniently used for P/S entry control to the output buffer. To avoid any 'race' conditions, the output buffer is then stored by $\overline{C}$ which has a single positive-pulse-edge transition occurring mid-way through the FFC7 pulse period (cf. fig. 3.3.2 above).

The relationship between FFC7 and the output bit stream is illustrated by the oscilloscope traces of fig. 3.5.2. It can be seen from fig. 3.5.2a that the first bit of each word (in this case the FS word and 14-bit data words corresponding to the 7-bit binary code '1111111') is clocked out in the middle of each FFC7 pulse period. Fig. 3.5.2b shows the inclusion of the FS word every sixth FFC7 pulse, this being the desired channel commutation rate.

The serial output of the buffer shift register provides the binary data for r.f. transmission. In view of this, the shift-register output drives a COS/MOS non-inverting buffer amplifier [8] which then provides a suitable interface to the transmitter frequency controlling device. [This interface is considered in the next section.]

3.6 The radio frequency transmitter circuit

In chapter 1, bio-telemetry was defined as the science of transmission of biological information to accessible locations. The techniques described in the previous sections of this chapter change the biological information signals into a form suitable for r.f. transmission from one location to another. An r.f. transmission link intended for use with low-power, near-field, implanted telemetry sources has been previously developed for a PDM/FM telemetry system[5].

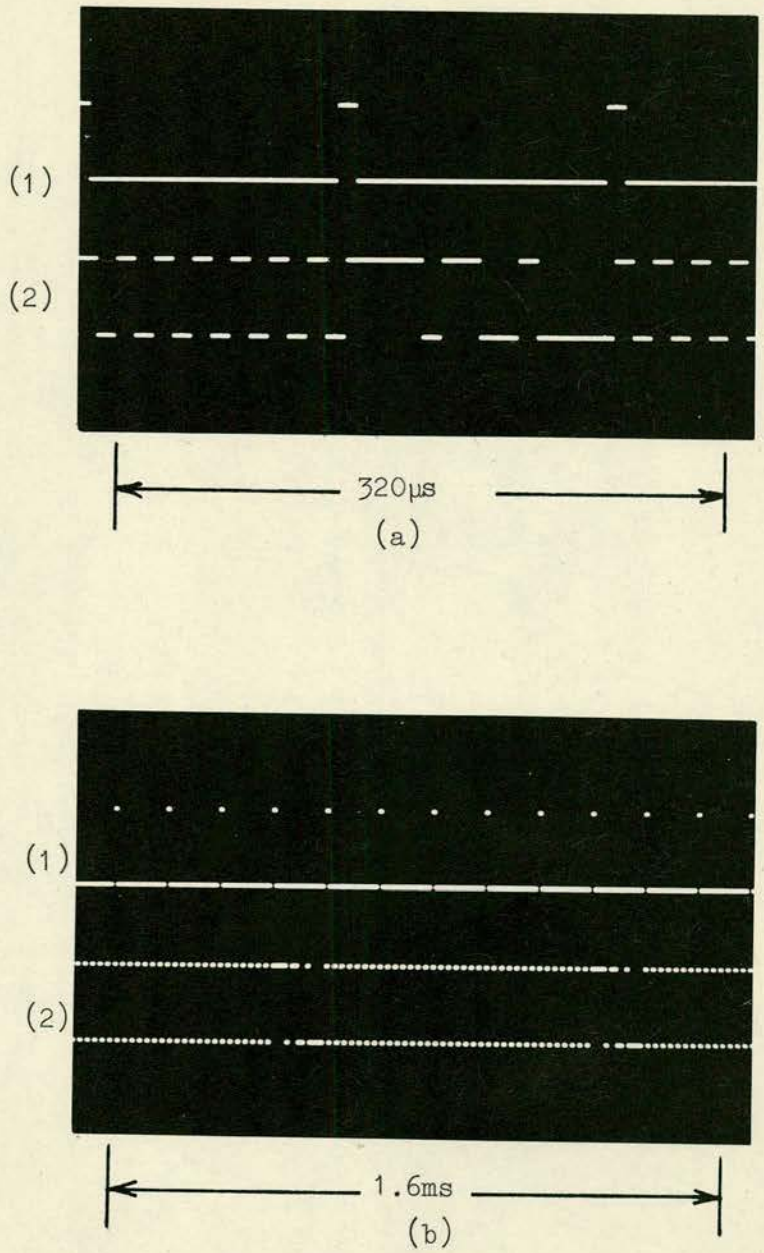


FIG. 3.5.2 Oscilloscope traces showing the relationship between

(1) the P/S control function, and

(2) the output bit stream with the maximum signal level applied to each data input channel.

The r.f. transmitter source of that system is fabricated as a thin-film circuit and, in accordance with the proposal of sect. 1.5 (viz. that this prototype transmitter source should be built using an existing thin-film transmitter circuit), it is considered here as a continuous-wave binary FSK source.

The circuit diagram of the thin-film r.f. transmitter is given in fig. 3.6.1. In order to minimise the size of the larger discrete components required to be bonded to the thin-film substrate (viz. the varactor diode, the oscillator capacitance and inductance, and the antenna tuning capacitance) the carrier frequency is made as large as possible. The frequency chosen is 27MHz which verges on the upper limit[24] (viz. 30MHz) of the allowed transmission band.

Oscillator tuning is achieved by varying the d.c. bias on the varactor diode. The stability of the carrier frequency is directly dependent upon the quality of the power-supply voltage, since extra voltage-controlling circuitry is unsuitable for an implantable circuit (cf. subsection 3.3.3 above). For implantation, the power-supply comprises a series of mercury watch cells[63] which produce a one per cent reduction in carrier frequency corresponding to a well-defined ten per cent reduction in voltage level during their effective working life. However, since r.f. tuning and AFC are readily implemented in the receiver (cf. section 4.2 below), this amount of variation in carrier frequency is acceptable in practice.

The accuracy of the frequency separation control is also dependent upon the variations in power-supply voltage.

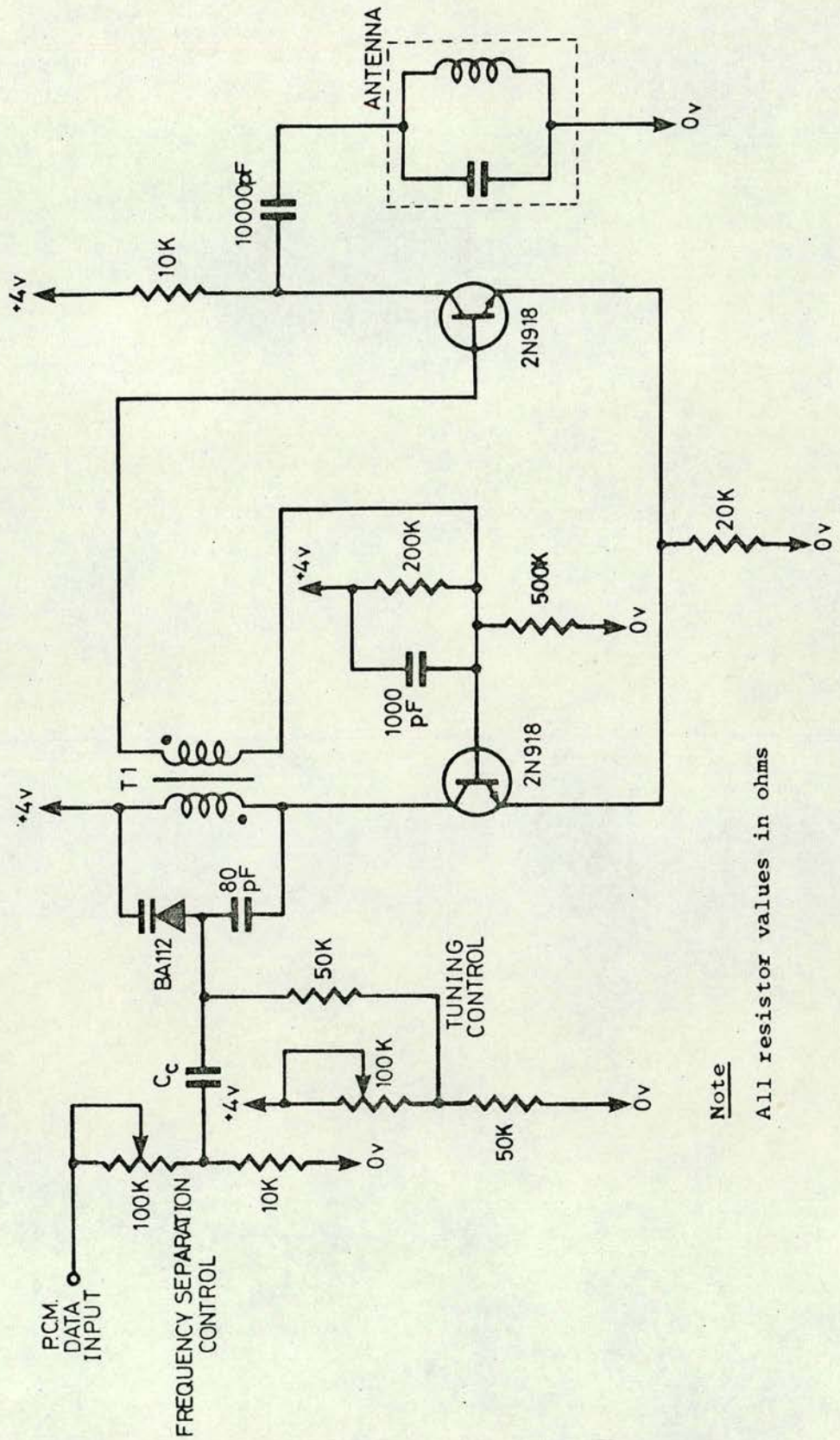


Fig. 3.6.1 The r.f. transmitter circuit.

Specifically, the difference in voltage level associated with the binary digits is defined by the output swing of a COS/MOS buffer amplifier (cf. sect. 3.5 above) which is virtually the same as the power supply voltage[8]. Although the required modulating signal voltage level is approximately five per cent of the power supply voltage[5], the per-centage accuracy in the resulting frequency separation remains the same as the per-centage accuracy of the power supply voltage (viz. ten per cent as noted above). In anticipation of this, the desired frequency separation may be initially preset to a larger value thereby defining the per-centage accuracy to be within ± 5 per cent overall. Such a variation has been shown (cf. sect. 2.5 above) to effectively reduce the performance of the telemetry system by at most 0.1 dB in γ_r (the received signal-to-noise ratio). Since this effective reduction in performance is negligible in comparison with an expected variation of 1dB in received signal power (cf. subsection 4.2.5 below), the ± 5 per cent accuracy of the frequency separation control is considered to be acceptable in the present system.

Two practical points in the design of the frequency-separation control are worthy of comment here:-

(i) The output impedance of the variable-resistance control and the capacitive load in the oscillator tank circuit have a low-pass filtering effect on the modulating waveform. In the present system, however, the output impedance of 1KΩ and capacitive load of 80pF give a time constant of 80ns which is negligible in comparison with the transmitted bit period of 10μs.

(ii) The output of the frequency-separation control is capacitively coupled to the oscillator tuning circuit. Bearing in mind that such capacitor coupling is to be avoided in situations where the average value of the binary data is likely to vary (cf. sect. 1.4 above), we note that it is acceptable in the present system since the balanced code to be transmitted ensures that each binary symbol occurs with the same relative frequency.

In view of (i) above, the frequency-modulating waveform effectively retains a rectangular pulse profile and the spectrum of the resulting FSK signal may be calculated accordingly. Since the balanced-code data to be transmitted are essentially of a random nature, then an average-power spectral distribution can be defined[27,28] which gives the best indication of the minimum system transmission-bandwidth requirements. The average-power spectrum $W_s(\omega)$ of a continuous-wave binary FSK signal is given by

$$W_s(\omega) = \frac{T}{4}\left[Sa^2\{(\omega+\omega_2)T/2\} + Sa^2\{(\omega-\omega_2)T/2\} + Sa^2\{(\omega+\omega_1)T/2\} + Sa^2\{(\omega-\omega_1)T/2\}\right] \quad .....(3.6.1),$$

where r is a dummy variable, T is the balanced-code bit period, ω_1 and ω_2 are the binary keying frequencies and

$$Sa(x) \equiv \sin x/x \quad .....(3.6.2).$$

[Appendix 3 refers.] By inspection, $Sa^2(x) < 0.01$ for $x > 10$.

Accordingly, the one per cent spectral bandwidth B_r (defined for $W_s(\omega) > 0.01$) may be given by

$$B_r \approx \{40 + (\omega_2 - \omega_1)T\} / 2\pi T \qquad (\omega_2 > \omega_1) \qquad \ldots\ldots(3.6.3).$$

The choice of keying frequencies ω_1 and ω_2 is dependent upon the receiver filter implemented (cf. sect. 2.5 above). In this prototype system, a critically-coupled band-pass filter is implemented; for which $(\omega_2 - \omega_1)T/2\pi = 1.26$ (cf. subsection 4.2.1 below), so that with $T = 10\mu s$, we have $B_r = 770KHz$.

In practice, however, the total required transmission bandwidth (comprising the spectral bandwidth component B_r and a component representing the expected drift in carrier frequency) is the important parameter in the design of the r.f. transmission and reception antennas. The transmitter antenna is of immediate interest, and (from fig. 3.6.1) it can be seen to be the inductance coil of a tuned-tank circuit. Obviously, the transmitter performance will be severly degraded if the carrier frequency drifts outwith the bandwith of the tank circuit.

In anticipation of the one per cent reduction in carrier frequency (as discussed above), the carrier frequency may be set initially high thereby defining an overall drift in carrier frequency of within one per cent (= 270 KHz). Accordingly, the total required transmission bandwidth is 1.04 MHz [= (270 + 770)KHz]. For the prototype system, a Q-value of 9 is chosen for the antenna circuit; this value being chosen since it defines a 3dB bandwidth of at least 3MHz/

3MHz and since, moreover, it ensures that the average power spectrum [defined above for $W_s(\omega) > 0.01$] is attenuated by no more than 10 per cent during the transmission process.

The foregoing discussion demonstrates that the thin-film r.f. transmitter circuit of fig. 3.6.1 is suitable for the transmission of the continuous-wave binary FSK signal. The design analysis of the prototype telemetry source is thus completed.

CHAPTER 4

THE DESIGN OF THE DIGITAL BIO-TELEMETRY RECEIVER SYSTEM

4.1 General

In this digital-telemetry system, the receiver function is essentially to detect shifts in the transmitted frequency and to convert these shifts into a corresponding digital form which is acceptable for output to some data storage/compression device. A block diagram of the basic system isgiven in fig. 4.1.1. It comprises four main blocks of circuitry, viz.

(i) the FSK detector to detect shifts in the transmitted frequency,

(ii) the bit-synchronisation circuit to isolate the transmitted bit rate for the synchronous regeneration of the received data from the detected shifts in frequency,

(iii) the bit-decision circuit to regenerate the binary data from the detected shifts in frequency by deciding upon the presence of a particular bit at a time synchronised with the end of the bit period, and

(iv) the frame-synchronisation circuit to isolate the FS word and synchronise the transfer of data to an output device for further processing.

Before discussing the design of the telemetry receiver in detail, it is useful to reviewthe two basic design criteria which are

(a) that the cost of producing the receiver should not be excessive since it is to be expected that more than one message source will be monitored simultaneously (thereby requiring more than one receiver),

and/

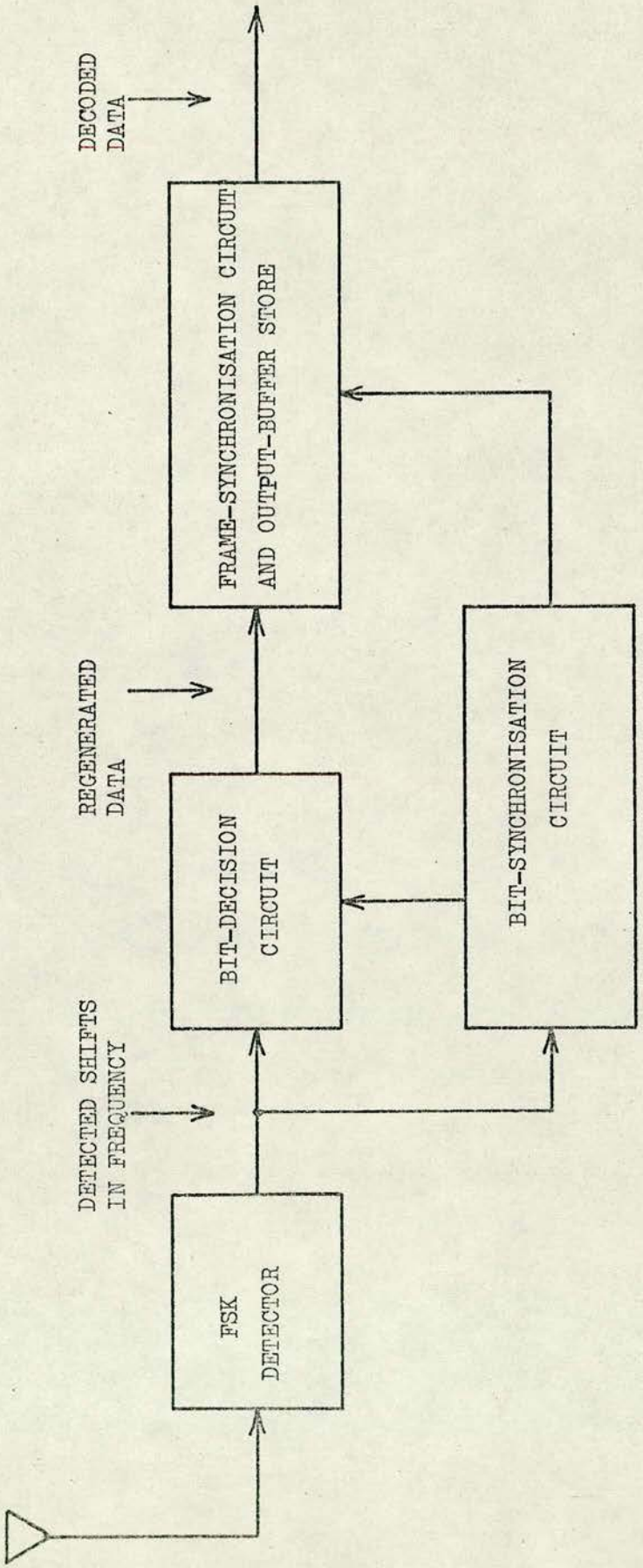


Fig. 4.1.1 Block diagram of the prototype receiver system.

(b) that the receiver should be easy to operate since it will normally be used by personnel not skilled in electronics.

The design of the telemetry receiver to meet these criteria is discussed in the following sections of this chapter. [Fig. 4.1.1 refers.]

4.2 The FSK detector

The discussion in chapter 2 has shown that a narrow-band filter with discriminator detection is to be preferred for the detection of continuous-wave binary-FSK data. However, in view of an expected drift in carrier frequency f_r of around 300KHz (cf. sect. 3.6 above), which is of the same order as the filter bandwidth required for a transmitted bit frequency of 100KHz in the present prototype system, practical implementation of this detection technique requires an r.f. tuner, narrow-band filtering then being achieved in the i.f. amplifier.

An i.f. frequency f_i of 2.5MHz is chosen so as to satisfy the band-pass filter symmetry requirements discussed in sect. 2.4 (according to which $f_i > 10\ B_3$). Down-conversion of f_r(= 27MHz) to 2.5MHz is achieved with a local oscillator frequency f_o centred, in this case, on 29.5MHz. In view of design criterion (a) given in sect. 4.1, however, the local oscillator tuning range is designed to be of the order $\pm$ 3MHz, which facilitates the selective monitoring of any one of several message sources frequency multiplexed in the band 24-30 MHz for simultaneous r.f. transmission. The 6MHz tuning range is obtained by utilising a self-excited L-C oscillator and the choice of high-side-beat frequency conversion (i.e. $f_i = f_o - f_r$), whilst introducing a frequency inversion, reduces the design constraints associated with such a wide tuning range.

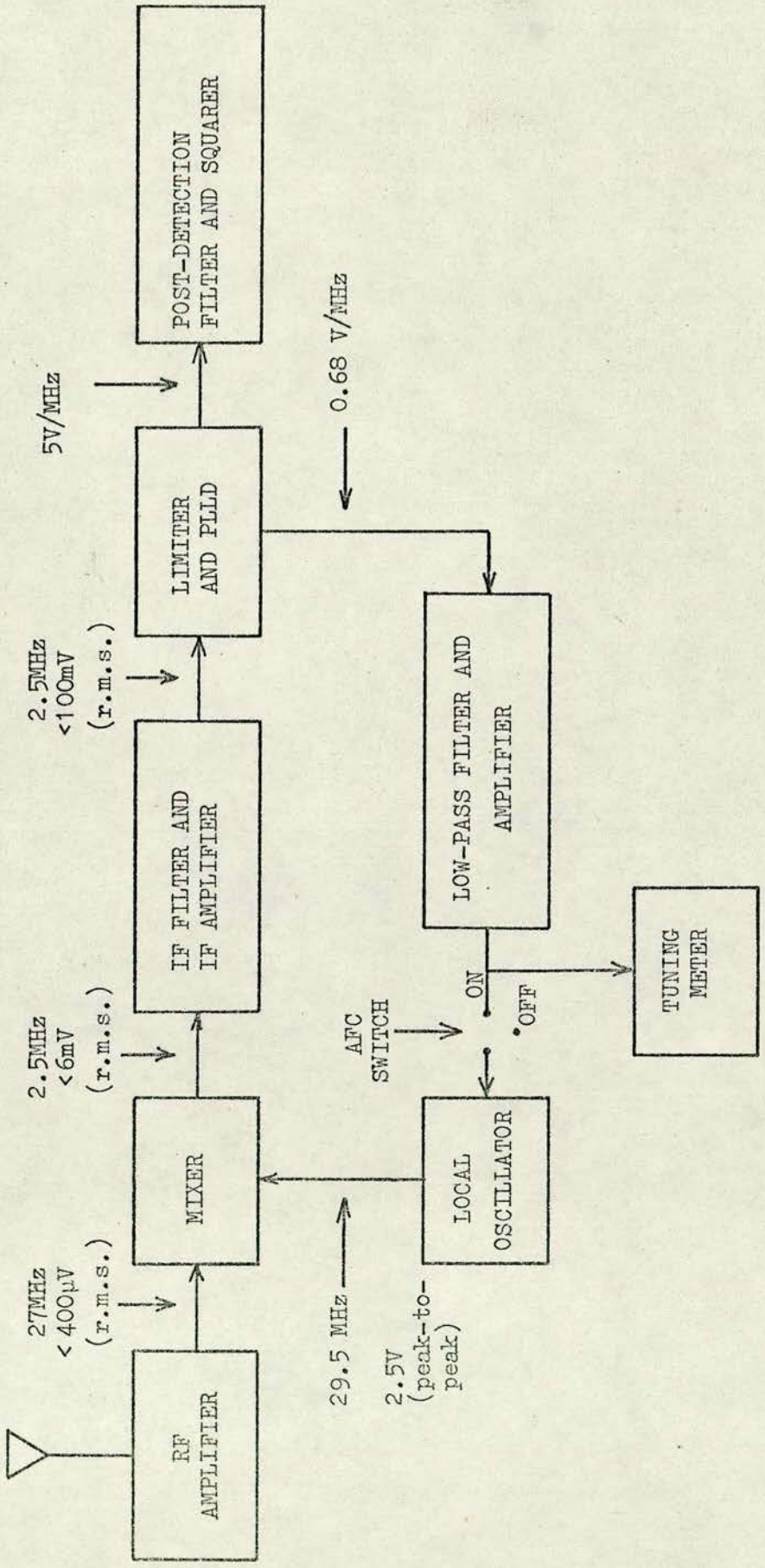


Fig. 4.2.1 Block diagram of the FSK detector.

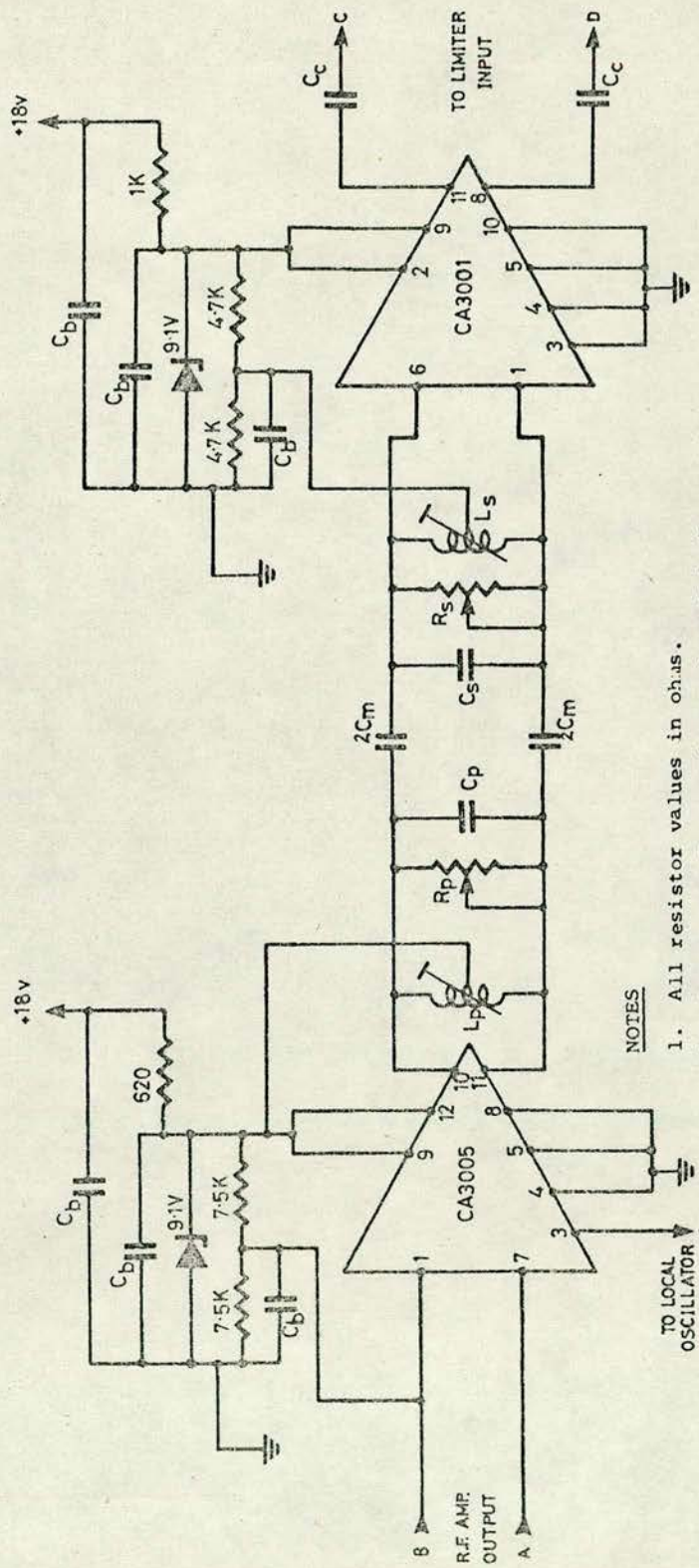
At these telemetry frequencies, however, self-excited L-C oscillators are subject to drift and short-term frequency instability which could be particularly troublesome in the present narrow-band system, the frequency conversion process producing a greater percentage variation at the lower i.f. frequency. AFC (automatic-frequency-control) circuitry is incorporated to combat such unwanted variations in f_i. [An analysis of the AFC is given in appendix 4.]

A block diagram of the complete FSK detector is shown in fig. 4.2.1. It will be noticed that the structure of the FSK detector is essentially the same as that of a conventional FM receiver. Indeed, the specification of the two systems would be identical except for the i.f. and post-detection filters. For FM reception the i.f. filter must be wide enough to accept the FM spectrum and the post-detection filter must provide the major filtering effect, the requisite cut-off frequency being the highest expected modulation frequency. For the FSK detector, on the other hand, the predominant filtering action is from the i.f. filter, the post-detection filter being used to remove unwanted harmonics at the output of the phase-locked-loop demodulator (implemented in view of the discussion in sect. 2.3).

The design and operation of the FSK detector is considered in the following sub-sections. [Fig. 4.2.1 refers.]

4.2.1 The mixer, i.f. filter and amplifier

The circuit diagram of the mixer, i.f. filter and amplifier is given in fig. 4.2.2. The integrated circuit amplifiers CA3005 and CA3001 are used respectively for the mixer and the i.f. amplifier. These devices are chosen for three reasons, viz.



NOTES

1. All resistor values in ohms.
2. All C_b and C_c capacitor values 0.1 μF
3. Rs and Rp are 10K multiturn potentiometers.
4. $C_p = C_s = 480$ pF; $C_m = 36$ pF.
5. Lp and Ls are bifilar wound variable inductors with a range 7-9 μH.

Fig. 4.2.2 Circuit diagram of the mixer, i.f. filter and i.f. amplifier.

(i) their suitability for operation at the r.f. and i.f. frequencies,

(ii) their performance is well specified, and

(iii) they provide common-mode rejection of unwanted signals when used differentially.

In the operating mode shown, the CA3005 amplifer facilitates multiplicative mixing [64] between the r.f. and local-oscillator frequencies, thereby producing signals at the sum and difference frequencies. Due to device nonlinearities, other spurious signals are produced, but these are of little consequence in the present system, since the i.f. filter rejects all frequency components except the required difference frequency.

For test purposes, it was decided to implement a critically-coupled tuned i.f. filter. The 3dB bandwidth and keying frequency separation requirements for optimum discriminator detection of binary FSK with such a filter system have been derived previously (cf. chapter 2 above). In particular, the 3dB bandwidth B_3 is specified in terms of the transmitted bit period T by the relationship

$$B_3T = 1.25 \ (=m_{c3}) \qquad .....(4.2.1)$$

(table 2.6.1 above refers), whilst the frequency separation $2\Delta f_d$ is specified with respect to B_3 by the relationship

$$2\Delta f_d/B_3 = 1.0 \ (= D_{opt}) \qquad .....(4.2.2)$$

(table 2.5.3 above refers). For the present system with T=10μs (cf. sect. 3.3 above), we have $B_3 = 2\Delta f_d = 125$KHz.

The filter thus specified is implemented by means of capacitive top coupling, this technique being chosen in preference to mutual-inductive coupling so as to give a finer control over the value of coupling coefficient. A mathematical analysis of capacitive top-coupling is given in appendix 5 from which the relevant design equations, for critical coupling at the resonance frequency f_c, may be summarised as follows:

$$\underset{\sim}{v}_s/\underset{\sim}{i}_r = j\tfrac{1}{2}\sqrt{(R_s R_p)} = j/4\pi f_c C_m \qquad .....(4.2.3),$$

$$\underset{\sim}{v}_p/\underset{\sim}{i}_r = Z_{in} = R_p/2 \qquad .....(4.2.4),$$

$$Z_o = R_s/2 \qquad .....(4.2.5),$$

$$B_3 = f_c^2\left\{\sqrt{(2L_pL_s/R_pR_s)}\right\}2\pi \qquad .....(4.2.6),$$

$$f_c = 1\Big/2\pi\sqrt{\left\{L_p(C_m + C_p)\right\}} = 1\Big/2\pi\sqrt{\left\{L_s(C_m + C_s)\right\}} \qquad .....(4.2.7);$$

where the components R_p, R_s, L_p, L_s, C_p, C_s, C_m are as shown in fig. 4.2.2, Z_{in} is the filter input impedance, Z_o is the filter output impedance, and $\underset{\sim}{v}_s/\underset{\sim}{i}_r$ is the phasor representation of the filter forward transfer impedance.

For this design $R_s = R_p$, and, in view of the inverse proportionality relationship with C_m [cf. with (4.2.3) above], the most convenient value of R_p is found to be 3.6KΩ. The resulting filter input impedance of 1.8KΩ (= $R_p/2$), together with a local-oscillator signal level of 2.5 volts peak-to-peak gives a mixer-stage gain of 15. [A local-oscillator signal of 2.5 volts peak-to-peak minimises the mixer noise figure and may be obtained practically without screening.] In the operating mode shown, the i.f. amplifier has a gain of 16 and thus defines a total voltage gain in the i.f. channel of 240 (= 16x15) or 47dB.

In view of possible future developments, such as the incorporation of AGC (automatic gain control) and a signal-strength meter, the maximum signal level at the output of the i.f. channel is specified as 100mV r.m.s. to avoid saturating the input of the following limiter stage (cf. subsection 4.2.2 below). Accordingly, the maximum signal levels allowed at the i.f. amplifier and mixer inputs are then 6mV r.m.s. and 400μV r.m.s. respectively.

4.2.2 The limiter and PLLD

The circuit diagram of the limiter-demodulator is given in fig. 4.2.3. The limiter comprises two RCA CA3001 integrated circuit amplifiers in cascade together with the differential amplifier input to the PLLD. In the operating mode shown, the voltage gain of the limiting amplifier is about 120 or 42dB.

The minimum signal level at the input to the PLLD to ensure saturation [65] is required to be 100mV r.m.s., which in turn defines the minimum signal level at the input to the limiting amplifier to be about 1mV r.m.s. Accordingly, the 100mV r.m.s. signal expected at the i.f. channel output (cf. subsection 4.2.1 above) is effectively hard-limited by this arrangement.

A Signetics NE562B general-purpose phase-locked-loop IC is used as the demodulator. In this system (with hard limiting of the input signal), the PLL has two very useful features, viz.

(i) the PLL open-loop gain is constant thus facilitating the specification of a set of fixed (i.e. signal-independent) closed-loop operational characteristics, and

(ii)/

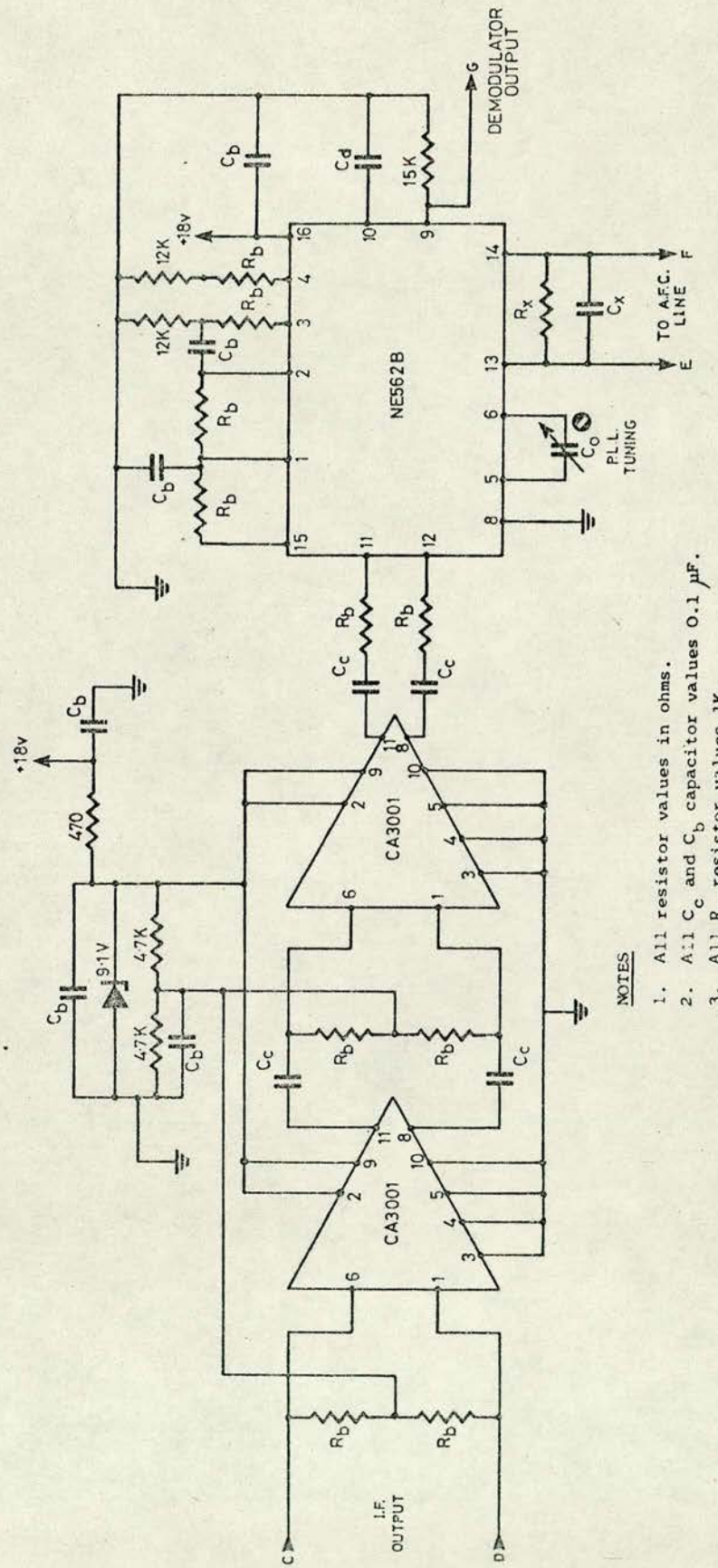


Fig. 4.2.3 Circuit diagram of the limiter and PLLD.

(ii) the loop phase detector has a linear transfer characteristic thus providing for linear frequency demodulation.

The desired PLLD operational characteristics have been discussed previously (cf. sect. 2.3 above) and are simply

(a) that the ratio of loop capture range to lock range should be approximately unity, thereby ensuring that the loop 'relocks' after an 'unlocking' transient [26,36], and

(b) that the demodulator should be broad-band in comparison with the i.f. filter bandwith.

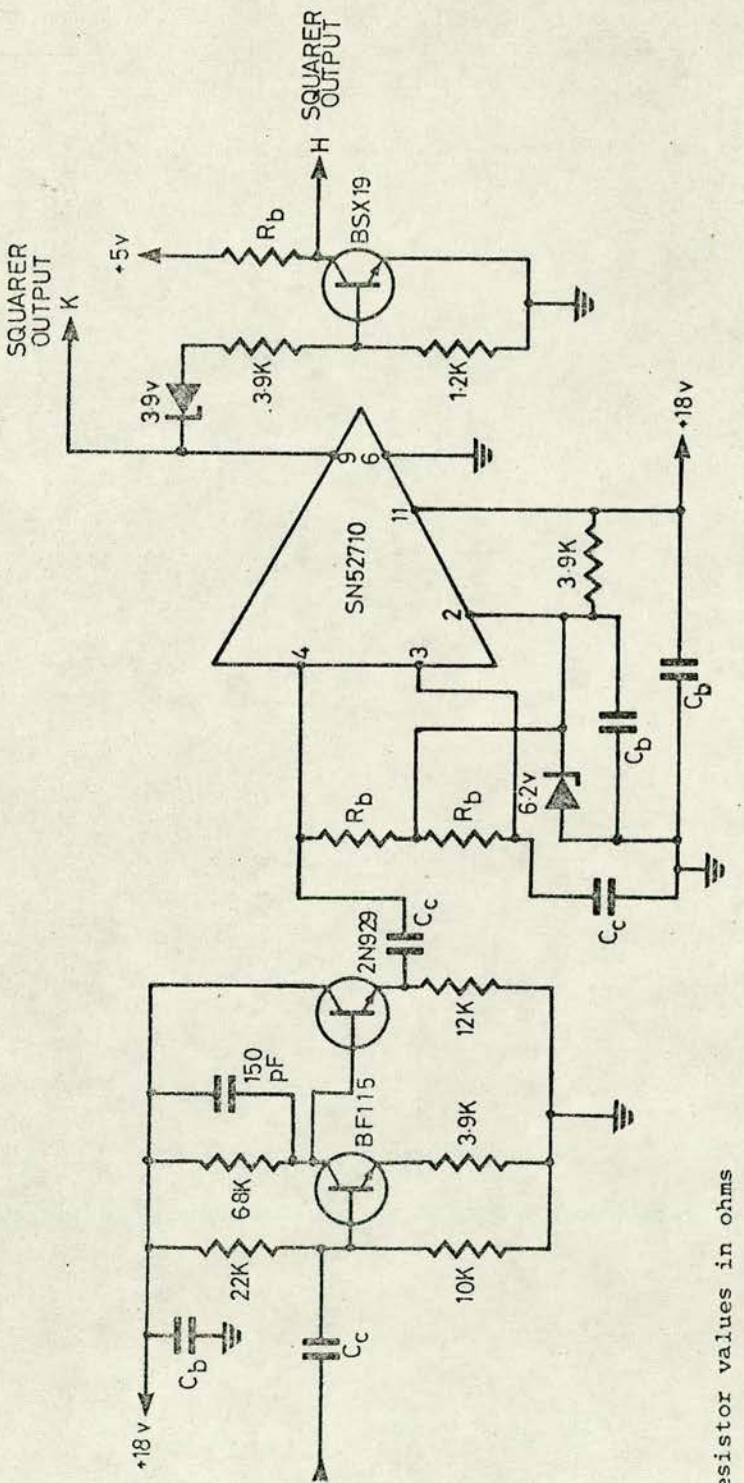
Requirement (a) is achieved by designing the PLL to have a second-order closed-loop transfer function with a damping factor greater [36] than 0.5. For requirement (b), the PLLD is designed to have a lock range of $\pm$ 300KHz centred on the i.f. frequency of 2.5 MHz.

It can be seen from fig. 4.2.3 that the PLLD provides both differential and single-ended demodulator outputs. The single-ended output (which has a sensitivity of 5V/MHz) is used as the normal demodulated output and drives the post-detection filter circuit whilst the differential output (which has a sensitivity of 0.68V/MHz) drives the AFC circuitry.

4.2.3 The post-detection filter and squarer

The circuit diagram of the post-detection filter and squarer is given in fig. 4.2.4. The function of the post-detection filter in this application is primarily to remove unwanted harmonics from the PLLD output. It was found that these distortion components could be successfully filtered by the single-stage low-pass filter shown

(cf./



Notes

1. All resistor values in ohms
2. All C_b and C_c capacitor values 1.0 μF
3. All R_b resistor values 1K.

Fig. 4.2.4 Circuit diagram of the post-detection filter and squarer.

(cf. sect. 5.3 below). This filter has a time constant of 5μs and (in comparison to the i.f. filter) does not significantly filter the noise component in the demodulator output.

The output of the post-detection filter represents the detected FSK signal. This detected signal is squared for compatibility with the digital circuits required for further processing. A high speed integrated circuit comparator is used for squaring and a logic-level conversion stage ensures compatibility with TTL (transistor-transistor-logic) digital devices.

It is worth noting here that there is an inversion between the TTL compatible output and the output of the PLLD. This arrangement compensates for the inversion in frequency deviation produced by the high-side-beat mixing of f_i and f_o. The effects of this inversion must also be bourne in mind in the design of the AFC loop.

4.2.4 The AFC channel and local oscillator

The circuit diagram of the AFC channel and local oscillator is given in fig. 4.2.5. The local oscillator basically consists of an r.f. amplifier with mutual-inductive feedback in a tank circuit. Two separate varactor diode stacks in the tank circuit provide for oscillator tuning and AFC, their respective control circuits being isolated from the oscillator by low-pass filters.

In this system, the AFC control voltage is derived at the PLLD differential output and amplified using a differential operational amplifier arrangement [66] which also accommodates the AFC low-pass filter/

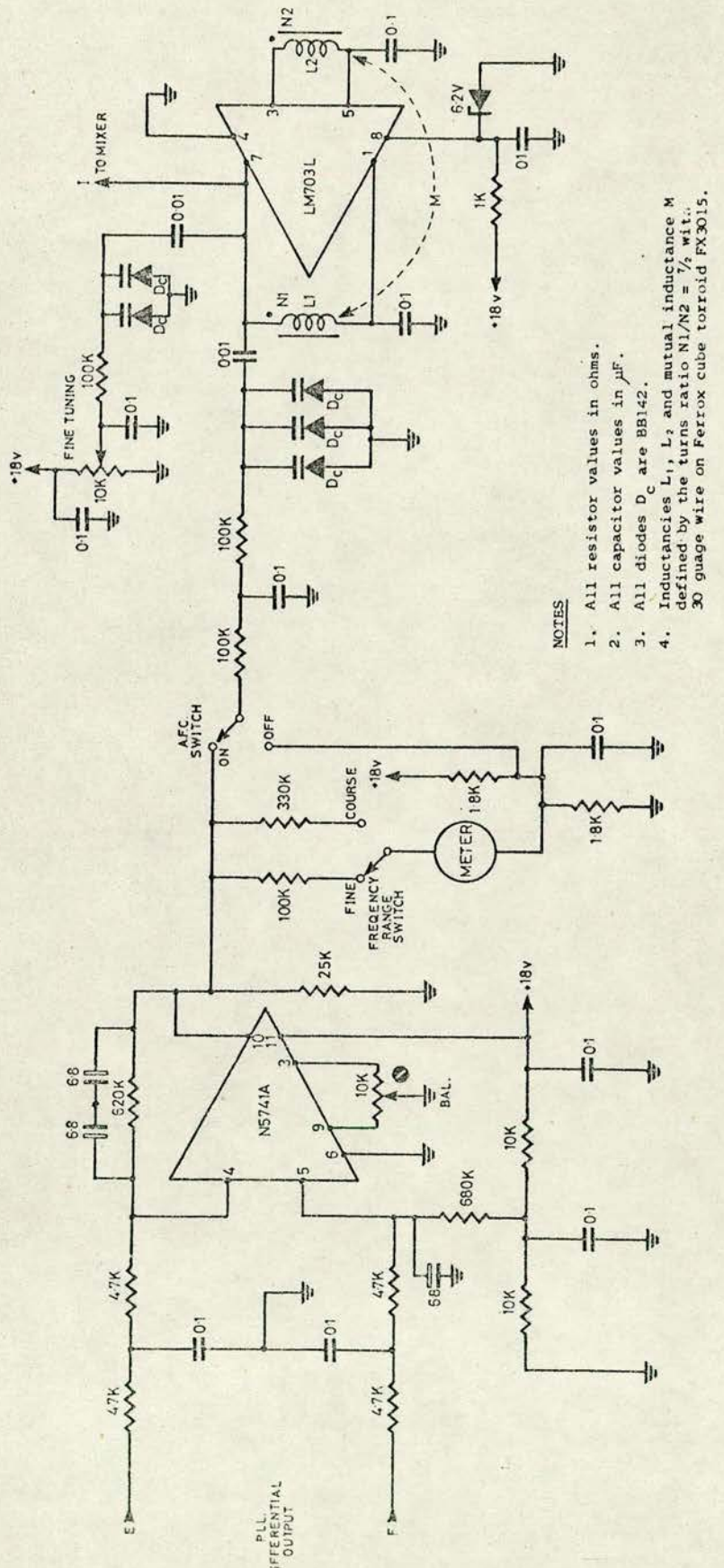


Fig. 4.2.5 Circuit diagram of the AFC channel and local oscillator.

filter (cf. appendix 4 below). In view of the extremely bad common-mode rejection properties of the operational amplifier at high frequencies, however, a low-pass filter was required to attenuate the high-frequency harmonic distortion in the PLLD output before amplification.

The single-ended output of the differential amplifier arrangement provides the automatic-frequency-control voltage. Accordingly, it is the most suitable position for inserting a centred-balanced meter and an automatic-frequency-control ON/OFF switch which facilitate detector tuning. In normal operation, the switch is opened for rough tuning and closed for fine tuning with the aid of AFC, the value of the i.f. carrier frequency being displayed at all times on the centre-balanced meter.

The relationships obtained in practice between f_i and the differential amplifier input and output voltages are illustrated by the curves of fig. 4.2.6. It can be seen that the input voltage is linearly dependent upon f_i within the range 2.2 to 2.8MHz, which is the lock range of the PLLD (cf. subsection 4.2.2 above). The output voltage is also linearly dependent upon f_i, but with a negative gradient and for the narrower tracking range 2.35 to 2.65MHz. [The negative gradient is required for AFC operation with high-side-heat mixing.] Accordingly, the AFC-loop lock range may be defined to be $\pm$ 150KHz with respect to the nominal i.f. centre frequency of 2.5MHz.

It is also useful to specify the AFC lock range with respect to f_r. This characteristic is found from the AFC closed-loop gain characteristic which is shown in fig. 4.2.7. It can be seen that the total lock range is around 9MHz but, due to the nonlinear capacitance-voltage/

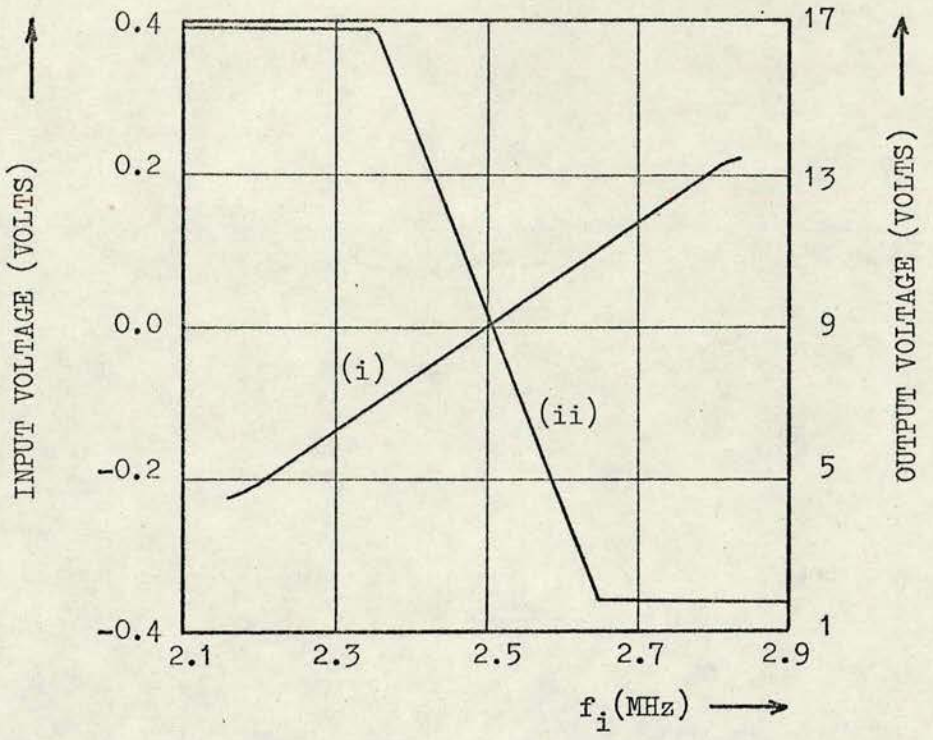


Fig. 4.2.6 The dependence of (i) the input voltage, and (ii) the output voltage of the AFC-loop amplifier on the i.f. frequency (f_i).

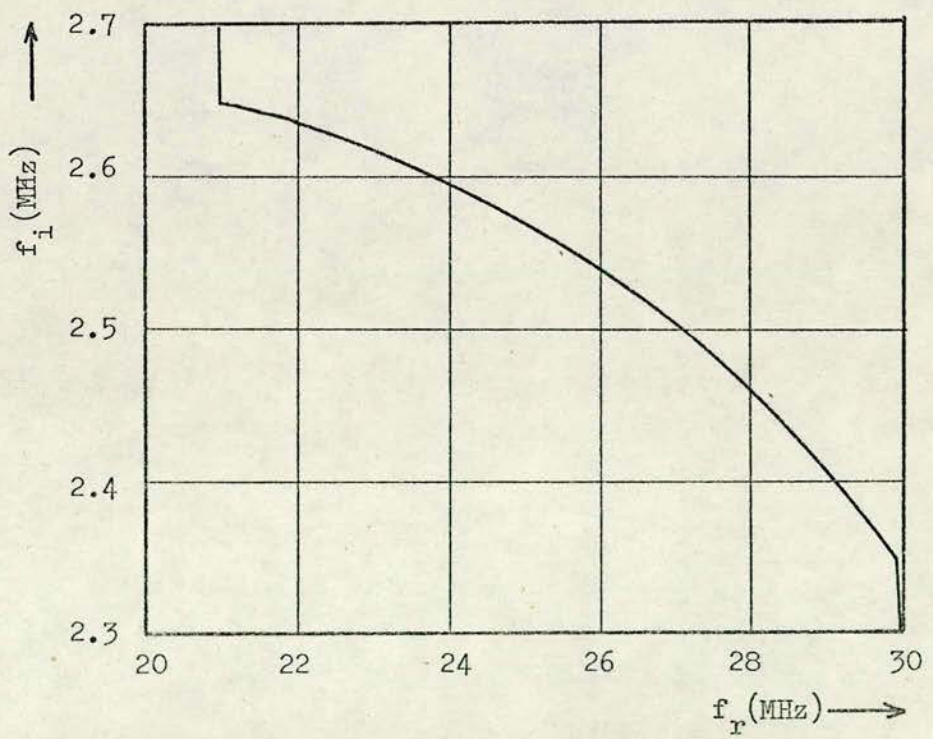


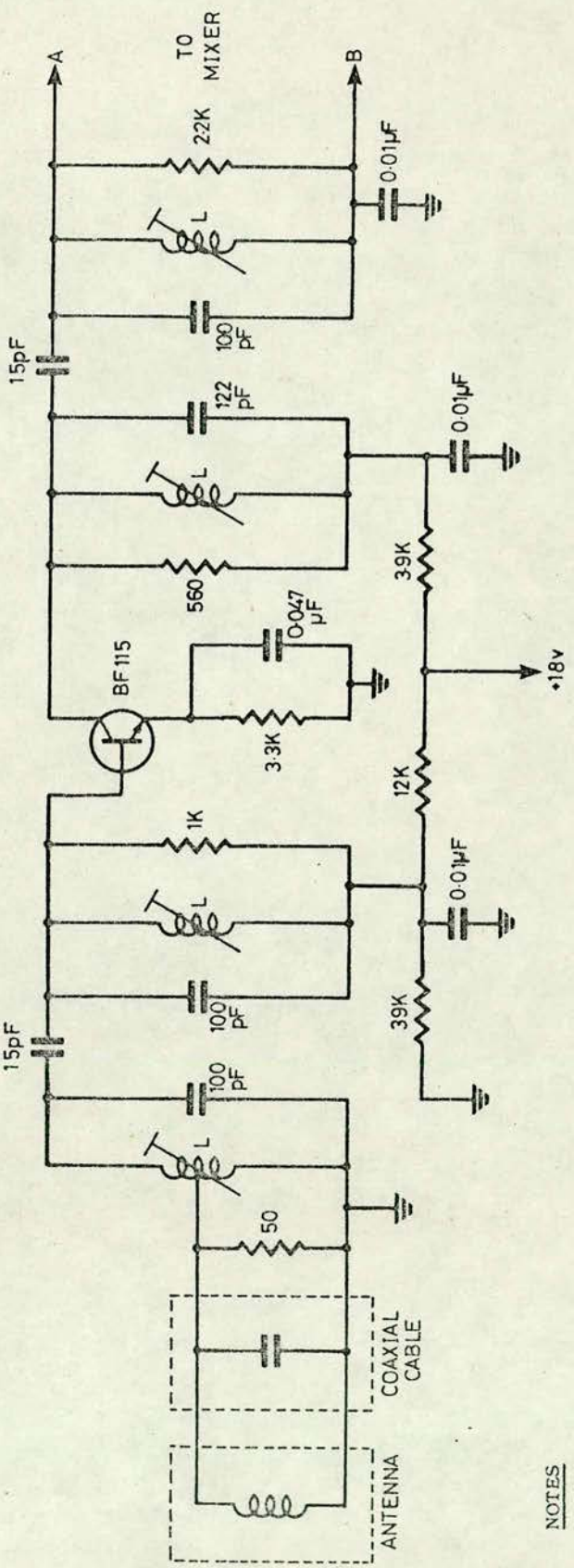
Fig. 4.2.7 Closed-loop AFC transfer characteristic.

voltage law of the varactor diodes, the variation about 27MHz is asymmetrical. However, for the expected drift in f_r of the order of $\pm$ 150KHz (cf. sect. 3.6 above), the characteristic is essentially linear and the analysis of AFC (given in appendix 4) holds accordingly.

4.2.5 The receiver antenna and r.f. amplifier

A receiver antenna and broad-band r.f. amplifier system have been developed previously [5] for use in low-power, near-field telemetry from an implanted source. Accordingly, this circuit was used to establish that the FSK detector would operate in an operational environment. [The operation of the FSK detector in an experimental environment is discussed later (in sect. 5.4 below).]

The circuit diagram of the existing antenna and r.f. amplifier is given in fig. 4.2.8. The antenna comprises a coil of wire encircling the cage of the animal being monitored. [Since the r.f. source is also a coil of wire (cf. sect. 3.6 above) the r.f. transmission path is essentially between the loosely coupled primary and secondary coils of an r.f. transformer.] The antenna coil is arranged for maximum signal pick-up which is estimated [25] to be at most 15μV r.m.s. in the present transmission link. It should be noted, however, that due to the animal's movement within the cage, the received signal power may be reduced by as much as 20 per cent or equivalently 1dB. The noise component in the received signal, on the other hand, remains constant and has an r.m.s. level estimated [25] to be about $0.008\mu V.Hz^{-\frac{1}{2}}$.



NOTES

1. All resistor values in ohms.
2. All inductors L variable 0.2-0.4 μH.

Fig. 4.2.8 Circuit diagram of the receiver antenna and r.f. amplifier.

The r.f. amplifier is a single-stage transistor amplifier which gives an r.f. stage gain of 25. This gain gives a maximum signal level at the mixer input of around 380μV r.m.s. which is less than the limit of 400μV r.m.s. set for normal operation (cf. subsection 4.2.1 above). The r.f. filter has a 3dB bandwidth of 1.5MHz which is broad enough to cope with the expected drifts in carrier frequency and also ensures that i.f. filtering is predominant. It should be noted, however, that this bandwidth is much less than the desired 6MHz receiver tuning range. The design of a more suitable r.f. stage is therefore required for the practical implementation of this receiver system.

From the received signal and noise levels specified above, the existing r.f. link is estimated to provide a received signal-to-noise ratio in the i.f. bandwidth of around 13dB. [This is a good estimate in practice since, at the telemetry frequency utilised here, the space radiation noise picked up by the antenna is significantly larger than the noise contributions of the active devices used in this receiver amplifier system [67].] We conclude this discussion of the FSK detector by noting that the signal-to-noise ratio of 13dB is significantly larger than the 7dB threshold value derived experimentally for the complete receiver system. [Sect. 5.5. below refers.]

4.3 The bit-synchronisation and bit-regeneration systems

The transmitted data consist of a series of balanced-code bits occurring at some bit rate which is constant (or approximately so). For the detection and further processing of the transmitted bits, it is necessary to have a receiver-based clock generator that is coherent with the bit rate. This clock must be derived from the transmitted data.

The average spectral density $W_d(\omega)$ of the transmitted balanced code data (assumed to be random for analysis purposes) is derived in appendix 6 and is rewritten here, as

$$W_d(\omega) = \lim_{N\to\infty} \frac{1}{N+1} \frac{1}{T} \sum_{r=0}^{N} \left\{ \omega^2 T^4 Sa^4(\omega T/2) \right\} \qquad .....(4.3.1).$$

From eqn. (4.3.1), it can be seen that there are no discrete frequency components present in $W_d(\omega)$. Specifically, there is no component at the bit rate and, moreover, $W_d(\omega)$ can be seen to have a null at the bit rate [i.e. substituting for the bit rate $f_b = 1/T$ gives $\sin(2\pi f_b T/2) = 0$, and consequently we have $W_d(2\pi f_b) = 0$]. Such a null in the spectrum of the transmitted data implies that the desired coherent clock waveform cannot be obtained by simply filtering the waveform of the received data.

In practice, the statistical properties of the transmitted data will be for the most part unknown (cf. sect. 3.1 above). However, since there is no definite indication that the data will not be random, we must assume here that it will be random and, accordingly, make provision for generating the required coherent clock from data whose spectrum has a null at the desired clock frequency.

In particular, we note that timing information in such a data signal is carried in the transitions between the binary digit levels, the times of transitions marking the boundaries of bit intervals. Transitions can have either positive or negative direction, but both polarities have the same meaning for timing recovery. If a series of unidirectional pulses is generated to mark transition times, there will be a discrete component of the bit frequency in this pulse train.

Accordingly, the received signal is first differentiated to mark the data transitions. The pulses of opposite polarity (obtained for positive and negative transitions) are then full-wave rectified to form pulses of the same polarity. These rectified pulses will have a discrete spectral component at the bit frequency which can be isolated by one of two methods:-

(i) By feeding the rectified pulse train into a tank circuit tuned to the bit frequency, the tank will resonate at this frequency and (provided the tank Q-factor is large enough) continue to resonate when no timing information is available.

(ii) By feeding the rectified pulse train into a PLL circuit centred on the bit frequency, the PLL will 'lock on' and (provided the loop bandwidth is small enough) maintain a signal with this frequency in the absence of timing information.

The bit-synchronisation process is complete when the coherent signal [obtained by either (i) or (ii)] is squared and phase-adjusted so that one edge of each pulse coincides with the end of the corresponding bit period in the detected FSK signal.

It has been noted (in subsection 3.3.1 above) that a variation of $\pm$ 1 per cent in the bit-rate is to be expected. The filter technique of (i) must therefore be broad-band enough to prevent such a variation causing comparatively large phase deviations (from the nominally tuned condition) of the clock-pulse waveform. The PLL technique [26] of (ii), on the other hand, has an extra facility that allows the tracking of slow drifts in the bit frequency whilst providing a narrow bandwidth. Accordingly, it is used in this application.

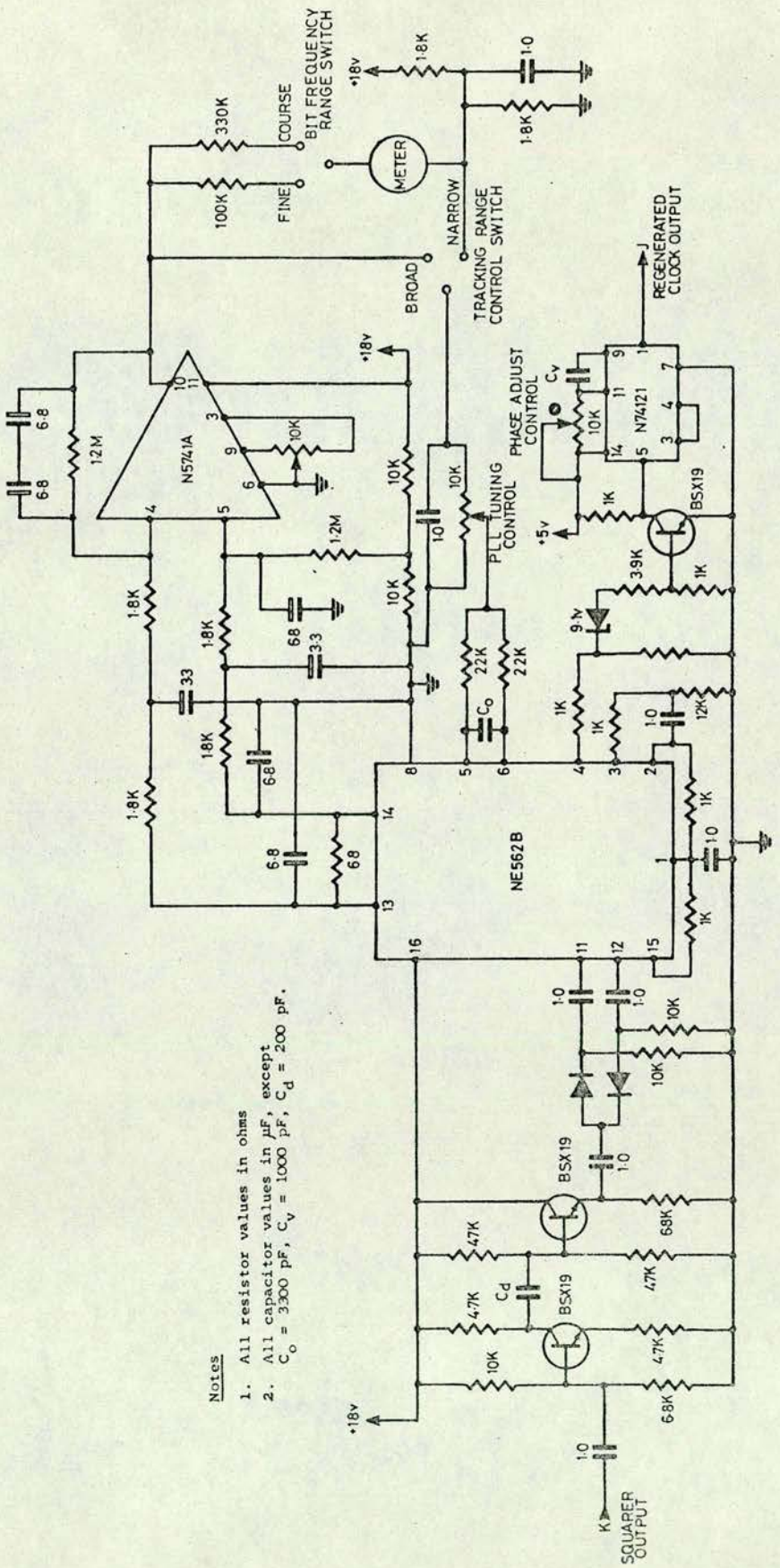


Fig. 4.3.1 Circuit diagram of the bit-synchronisation system.

The circuit diagram of the complete bit-synchronisation process is given in fig. 4.3.1. The signal input is derived at the squarer output in the FSK detection system. [Fig. 4.2.4 refers.] Differentiation is achieved by the coupling capacitor C_d in the first amplifier stage and produces bi-directional pulses of constant amplitude defined by the amplifier gain and the separation in voltage levels at the squarer output. The two diode-resistor combinations at the output of the amplifier produce parallel half-wave rectified pulses of opposite polarity which are then effectively combined to give pulses of the same polarity. This is achieved by the differential-input stage of the PLL integrated circuit device used here (viz. a Signetics [65] NE562B).

The relationships between the signals thus discussed (viz. the squarer, differentiator, and full-wave rectifier output signals) are illustrated by the oscilloscope traces of fig. 4.3.2 for the frame-synchronisation bit pattern appearing at the squarer output.

It should be noted that data extraction will eventually depend upon how well this system remains synchronised to the received data. Of particular importance in this connection are the PLL filter 'unlock' characteristics. It has been shown that rapid 'relock' (after an extraneous perturbation has caused the loop to become 'unlocked') is achieved [36,39,40] when the ratio of loop capture range to lock range is approximately unity. The PLL filter is designed to meet this criterion, accordingly.

In particular, the PLL functions of tracking and filtering are implemented in this system by two distinct feedback loops. The feedback/

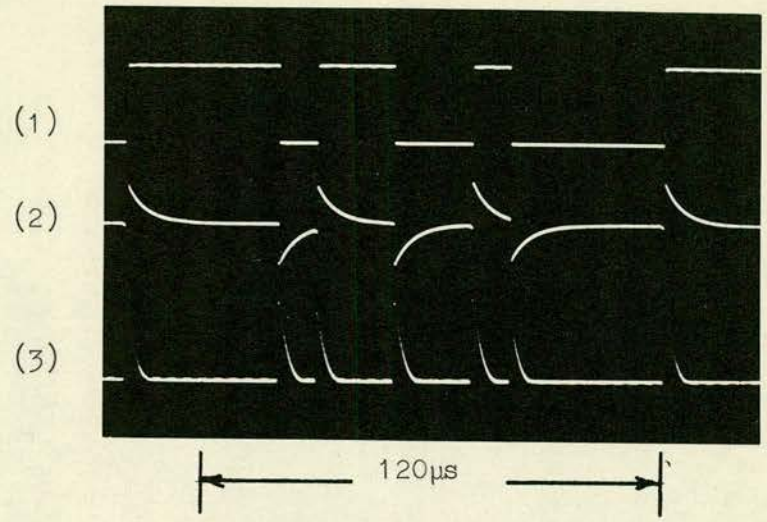


FIG. 4.3.2 Oscilloscope traces showing the relationship of

(1) the squared demodulated signal,

(2) the differentiated signal, and

(3) the full-wave rectified signal (PLL input signal).

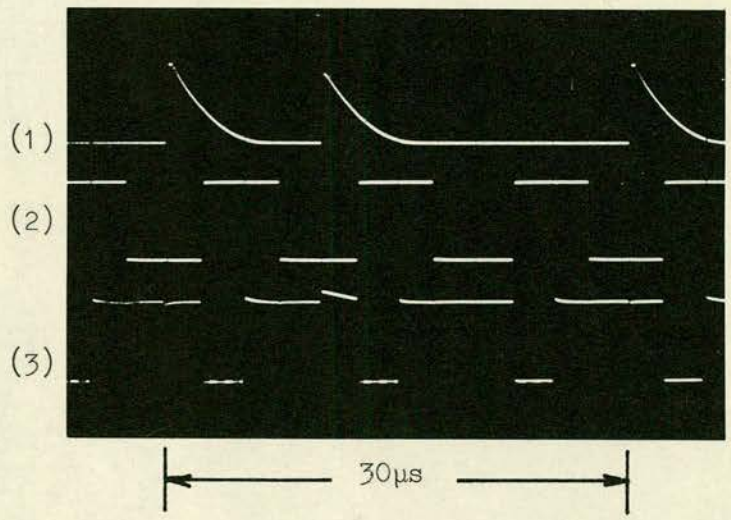


FIG. 4.3.3 Oscilloscope traces showing the relationship of

(1) the PLL input signal,

(2) the PLL output signal, and

(3) the monostable output signal.

feedback-loop normally utilised [65] (in the NE562B device) provides for a narrow-band filter with a lock range to capture range ratio of unity. The lock range of this loop is chosen to be ± 1 per cent of the bit frequency f_b since at lower values voltage drifts within the PLL device will reduce its operating performance [65].

A second loop, specifically via the differential amplifier circuit, facilitates the tracking of slow drifts in bit rate. In comparison with the previous loop described, this loop has an extremely narrow bandwidth and a much wider lock range (viz. ± 10 per cent of f_b) so that the maximum expected drift of ± 1 per cent in the transmitted bit-rate effectively produces only a ± 10 per cent change in the phase of the PLL output signal.

Initial tuning of this PLL circuit is most easily achieved by monitoring the tuning meter with the additional loop open-circuited. Once tuned, the additional loop is closed and the normal functions of filtering and tracking can then take place. The operation of this arrangement is the same as that of the discriminator-aided acquisition of lock described by Gardner [26]. The comparatively broad-band loop acts as a discriminator with a capture range of ± 1 per cent of f_b whilst the narrow-band loop acts as a conventional tracking filter. Essentially, the discriminator action ensures that whereas loss of lock is never permanent, it is achieved at the expense of a greater noise output power.

This PLL circuit provides a square-wave output signal, thus obviating the need for a special squaring device. On the other hand, it requires a logic level conversion stage to drive the TTL retriggerable monostable [68] used here for final phase adjustments of the regenerated clock waveform. In particular, the monostable output pulse period is synchronised with the end of the corresponding bit-period of the detected FSK signal. The oscilloscope traces of fig. 4.3.3 show the relationships obtained in practice between the PLL input signal, the PLL output signal, and the regenerated clock waveform appearing at the monostable output.

By using the monostable output signal to clock the value of the squared detected signal into a storage device, a decision on the presence of a certain bit is made at the point of maximum demodulated signal strength. The storage device can be considered to be part of the frame-synchronisation process (to be considered in the next section).

4.4 The frame-synchronisation system

A pulse communication receiver must perform two synchronisation functions before the data received can yield information [69,70]. Firstly, it must provide (as discussed in the previous section) a time base which can be used to determine the end of an individual bit period. Secondly, it must indicate the occurrence of a distinct pattern of bits inserted in the waveform at the transmitter for 'sorting' the various channels of data within a frame. This latter function is known as frame (or group) synchronisation.

In terms of modern information theory [69], the ideal frame synchronisation process is

(i) to store any number of complete frames of regenerated data,

(ii) to compute (from these stored data and also from the prior knowledge available about the FS word) the probability that the FS word is inserted at each bit position of the most recently received frame, and

(iii) to select on this basis the most probable position in which the FS word was inserted.

No amount of processing can do better. The ideal frame synchronisation process thus consists of a number of computations of probability made in parallel (as many as there are bit-positions within the frame) followed by a selection of the position whose probability is greatest.

The implementation of this ideal process was costed and found to be excessively expensive (mainly in consequence of the price of the large storage element required). It was decided, therefore, to adopt a more conventional frame synchronisation process.

The conventional approach to frame synchronisation is to set some threshold criterion on which to base the 'sync' decision and then to search serially through successive regenerated bit positions for a sequence of bits that meet this criterion. The bit position corresponding to the first sequence of bits to satisfy the criterion is then declared to be the sync position sought and the synchronisation process locks into that position. To aid this process, the FS word is usually constructed (as shown in sect. 3.2) in such a way as to minimize the probability that some other sequence of bits might be mistaken for this word.

A flow chart of the basic process adopted here is given in fig. 4.4.1. It can be seen that two operating modes can be defined, viz.

(i) the search mode, and

(ii) the sync mode.

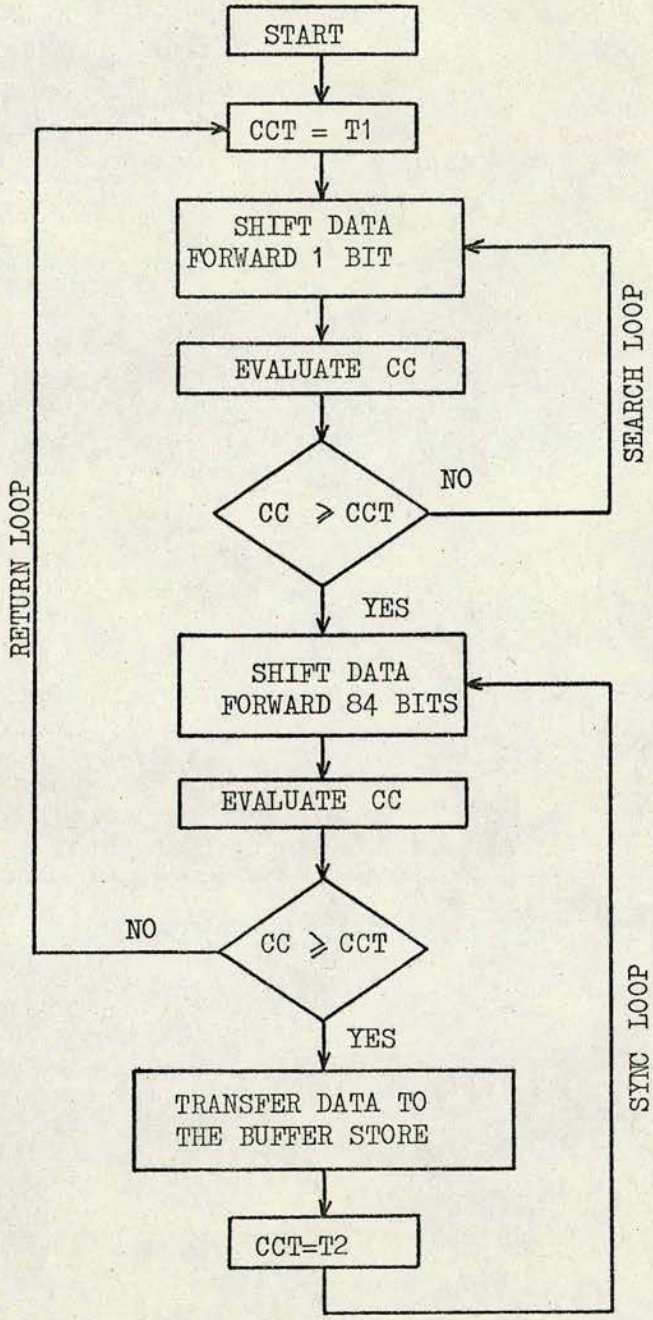
A transition between these operating modes is controlled by comparing the relevant coincidence counts (denoted here by CC) with a coincidence count threshold level (denoted here by CCT), each coincidence count being obtained by a comparison of the known FS word with the most recent 14 bits of regenerated data.

In the search mode, the value of CCT is set to T1 (say) and values of CC are obtained for each bit position of the data until the condition

$$CC \geqslant CCT \qquad \text{.....(4.4.1)}$$

is satisfied. Once this condition is satisfied the operation transfers to the sync mode.

In the sync mode, 84 data bits (i.e. one frame of data in the present trial system) are allowed to pass between obtaining values of CC and testing the condition (4.4.1). If such a sync-mode test is successful, the process continues to operate in the sync mode for another 84-bit period. The previous 84 data bits are then known to exist between two groups of bits satisfying the coincidence-count threshold and are transferred to an output-buffer store accordingly. Also, the value of CCT is reduced to T2 (say) for continuing operation in the sync mode.



CC denotes the coincidence-count value

CCT denotes the coincidence-count threshold value

T1 denotes the search-loop threshold value

T2 denotes the sync-loop threshold value

Fig. 4.4.1 Flow chart of the frame-synchronisation process.

If a sync-mode test is unsuccessful, on the other hand, the operation is returned to the search mode, no data are transferred to the output buffer store, and CCT is reset to T1.

The performance of this process is clearly dependent upon the choice of threshold settings for the search and sync modes. If the threshold values are set too high, a sync decision (i.e. the outcome of a successful sync test) may be delayed for an indefinite period of time during which all the data are lost. If the threshold values are set too low, then false sync decisions will occur at a high rate, and again all the data are lost.

It is shown experimentally (sect. 5.5 above refers) that a threshold value of γ_r (the received signal-to-noise ratio), above which there is no significant loss of frame synchronisation, can be defined for particular values of T1 and T2. Since the transmitted signal power is not at a premium in this telemetry system, it was decided that the particular threshold value of γ_r, corresponding to the choice of T1 and T2, should define the minimum received signal strength. In the present system, therefore, the values of T1 and T2 are chosen (bearing in mind the foregoing discussion) to combat the more practical problem of comparatively short-term increases in the error-rate of the recovered data caused by spurious noise sources (other than Gaussian) not considered in the theoretical analysis.

For the 14-bit transmission code of this system, the values of T1 and T2 are chosen as 13 and 11 respectively after consideration of the worst-case-data cross-correlation coefficients (listed in fig. 3.2.1 above). The value of 13 for the search-mode threshold level/

level T1 requires that at least three errors occur successively in the same worst-possible data word before a wrong sync decision is made. This choice also allows one error to be made in each correct FS word thus ensuring rapid synchronisation for normal operation. The choice of 11 for the sync-mode threshold T2 means that four errors must be made before an FS word is not acceptable, thus avoiding loss of lock except with extremely high error-rates. Moreover, this choice of T2 requires that at least one error be made in the same worst-possible data word continuously for a false synchronisation condition to be retained. False synchronisation is therefore unlikely to be prolonged in normal operation.

The frame-synchronisation process under discussion (fig. 4.4.1 refers) was built using TTL devices to make use of the variety of MSI-circuit modules now available [68,71]. A circuit/block diagram of the system implemented is given in fig. 4.4.2. An explanation of the operation of this system follows.

The regenerated data are clocked into a 16-stage serial-in/parallel-out shift register. In accordance with the discussion in sect. 4.3 above, the first stage of this shift register performs the bit-decision-making process since the binary value present at the data input is stored by a positive-pulse-edge transition of the synchronised clock waveform (denoted here by C). The first fourteen parallel outputs then represent the most recently recovered data and are compared with the FS word in the coincidence counter (to be discussed later). The last two-parallel outputs are compared in an EXCLUSIVE-NOR/

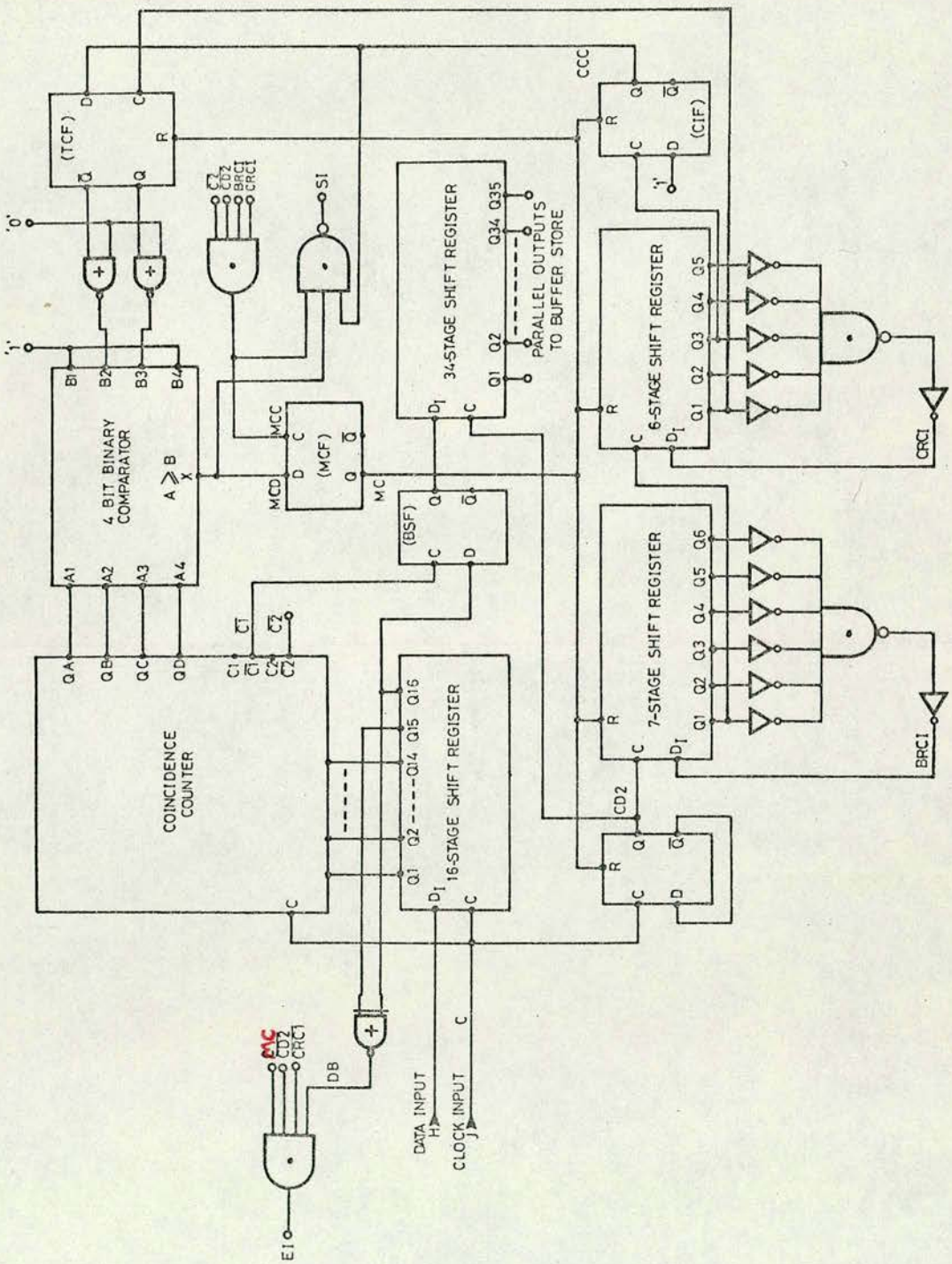


Fig. 4.4.2 A circuit/block diagram of the frame-synchronisation system.

EXCLUSIVE-NOR logic gate whose output (denoted here by the logic function DB) indicates the occurrence of the possible bit-error patterns '11' and '00' in the recovered data. [Sect. 3.2 above refers.] Accordingly, the output DB is utilised (as discussed later) to define errors in the regenerated data.

Once every bit period, the 4-bit binary comparator device compares the coincidence count with the coincidence-count threshold value, either T1 or T2 (as the case may be). The output of the comparator (denoted here by the logic function MCD) is clocked into a D-type flip-flop (MCF) whose output then represents the sync/search mode control function (denoted here by MC). If MC is '0', the system is considered to be in the search mode and each bit position is interrogated to find the synchronisation pattern. If MC is '1', the sync mode is operational and in this case, 84 bit positions are allowed to pass between tests for the synchronisation pattern.

The 84 clock pulses are counted in three stages:-

(i) A divide-by-two stage is clocked by the input timing waveform C. The output of this stage (denoted here by the logic function CD2) is used for clocking the regenerated data from the 16-bit shift register into a 34-bit shift register before being passed to the buffer store (to be discussed later). This divide-by-two process decodes the serial 14-bit balanced-code words into the corresponding 7-bit binary-code words before output processing, and thus saves storage capacity.

(ii) A self-starting ring counter divide-by-seven stage (referred to here as BRC) is clocked by CD2.

(iii)/

(iii) A self-starting ring counter divide-by-six stage (referred to here as CRC) is clocked by BRC, the first stage output of BRC.

This technique of counting simplifies the generation of three logic functions which depend on count position:-

(1) The clock-input function of flip-flop MCF (denoted here by MCC) is given simply by

$$MCC = CRCI.BRCI.\overline{CD2}.\overline{C2} \qquad .....(4.4.2),$$

where CRCI and CRCI are the decoded inputs to CRC and BRC respectively, and $\overline{C2}$ is a logic function generated in the coincidence counter. Essentially, the function $CRCI.BRCI.\overline{CD2}$ defines the occurrence of the 84th bit position in each regenerated frame of data, whilst the function $\overline{C2}$ ensures that the coincidence count is complete. An interesting design feature to note here is that if MC is '0' (thus indicating the search mode), the 'bit-counting' mechanism is constrained in the 84th bit position thereby allowing each regenerated bit position to be interrogated until the synchronisation pattern is found.

(2) The control function (denoted here by SI) for data transfer to the output buffer is given simply by

$$SI = \overline{MCC.MCD.CCC} \qquad .....(4.4.3),$$

where the logic function CCC (the output of flip-flop CIF) is '0' in the search mode and '1' for the continuation of the sync mode.

(3)/

(3) The function (denoted here by EI) indicating errors in the regenerated bit stream is given simply by

$$EI = \overline{CRC1}.\overline{CD2}.MC.DB \qquad .....(4.4.4),$$

where CRC1 denotes the first stage output of CRC. Essentially, the function $\overline{CRC1}.\overline{CD2}.MC$ ensures that the bit-error patterns indicated by the function DB (as discussed above) are restricted (a) to operation in the sync mode, (b) to the regenerated data words (i.e. the FS word is not monitored), and (c) to the correct phase position (i.e. after every two data-clock pulses). Although this function is not used here, it could be used as an extra control function (cf. sect. 3.2 above) in possible later systems.

The logic functions MC and CCC also control the coincidence count threshold value, either T1 or T2 (as the case may be). In the search mode, MC is '0' and the threshold-controlling flip-flop TCF is reset in order to define the binary equivalent of T1 with its parallel outputs (Q and $\overline{Q}$). In the sync mode, MC is '1' and the reset on TCF is lifted. If the sync mode is maintained CCC becomes '1' which is then clocked into TCF (by CRC1) thereby interchanging the values stored at its parallel outputs to define the binary equivalent of T2.

To conclude this discussion of the frame synchronisation process, the special devices, viz.

(i) the coincidence counter, and

(ii) the output buffer store,

are considered in turn.

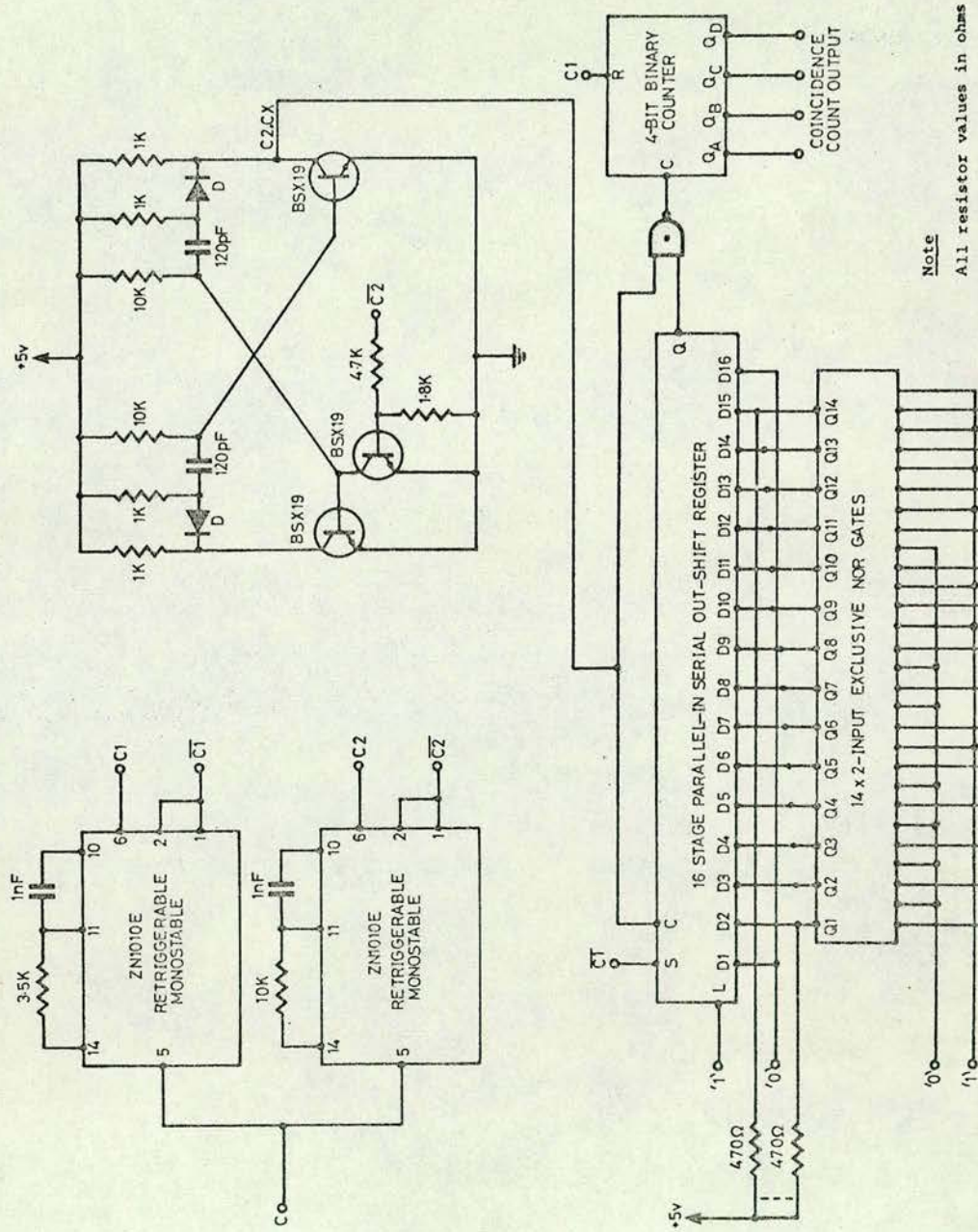


Fig. 4.4.3 Circuit diagram of the coincidence-count system.

4.4.1 The coincidence counter

The circuit diagram of the coincidence counter is given in fig. 4.4.3. This circuit has three basic operations, viz.

(i) the generation of a coincidence pattern by presenting the 14-bit data input and the 14-bit FS word as the parallel-inputs to fourteen 2-input EXCLUSIVE-NOR gates,

(ii) the storing of the coincidence pattern in a parallel-input/serial-output shift register, and

(iii) the clocking of the shift-register output into a 4-bit binary ripple counter thereby producing a binary representation of the coincidence count.

A gated astable multivibrator provides the high-frequency pulse waveform to clock the shift register. The minimum clocking frequency is obtained by considering the following design features:-

(i) At the start of each bit period, time must be allowed for the propagation delays to be expected in the generation and storage of the coincidence pattern. The time allowed for this process is governed by C1 which is derived from the clock input C by means of a retriggerable monostable. This same function is used to reset the 4-bit binary ripple counter in anticipation of the next count.

(ii) At the end of each bit period, time must be allowed for the comparison of the ripple counter output and the coincidence-count threshold value before the ripple counter is reset. The time allowed for this process is governed by C2 which, (like C1) is derived from C by means of a retriggerable monostable.

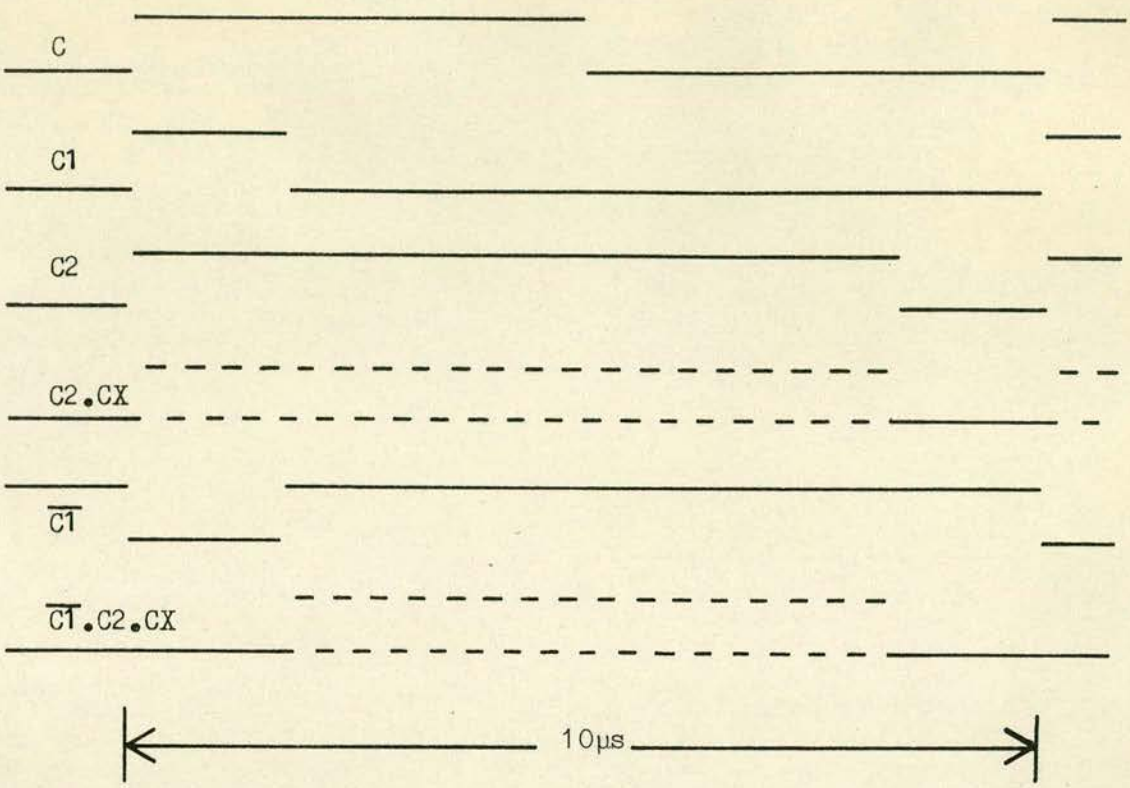


FIG. 4.4.4 Timing diagram of the coincidence count control functions.

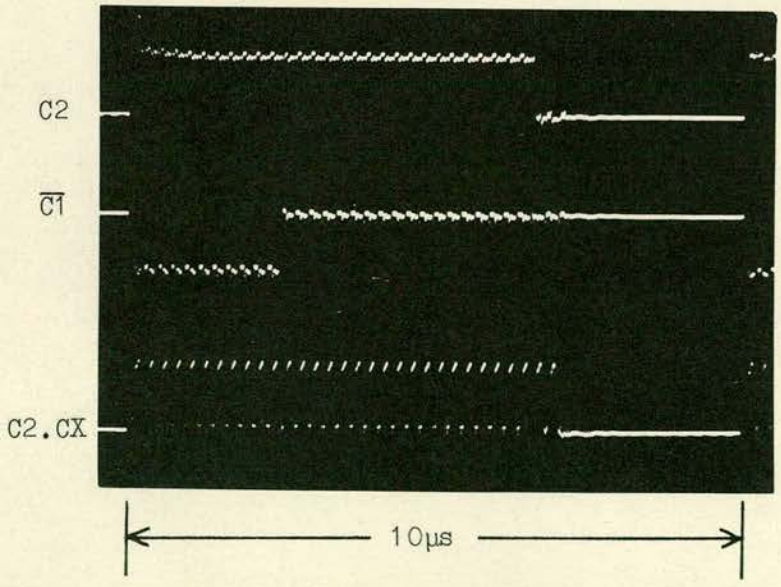


FIG. 4.4.5 Oscilloscope traces showing the relationships obtained in practice for some of the coincidence count control functions.

The time period defined as $\overline{C1}.C2$ is therefore used for counting the serial output pulses of the shift register. Since the bit period is 10μs in the present system, speed is not of great importance, and the only design criterion is that the frequency of the multivibrator should be large enough to allow at least fifteen timing pulses within the $\overline{C1}.C2$ pulse period.

A timing diagram of these control functions is given in fig. 4.4.4. The astable multivibrator is gated by $\overline{C2}$ and the resulting timing function is termed C2.CX, where CX can be considered to be a free-running multivibrator output synchronised to the input clock. The oscilloscope traces of fig. 4.4.5 illustrate the relationships obtained in practice between some of these control functions.

4.4.2 The output-buffer store and channel multiplexer

The regenerated data, held at the serial-input and in the parallel-output stages of the 34-stage output shift register (shown in fig. 4.4.2), are transferred to an output-buffer register on receipt of the negative-pulse-edge transitions of the logic function SI [defined in eqn. (4.4.3)]. Normally the outputs of the buffer register could be grouped for separate channel outputs. In this case, however, these groups are multiplexed for output to a single processing unit, e.g. a computer.

The circuit diagram of the output buffer store and multiplexer is shown in fig. 4.4.6. A channel selected for output is isolated by means of the logic functions CSx (x = 1 to 5). In particular, a '1' on the channel select function corresponding to the data of interest/

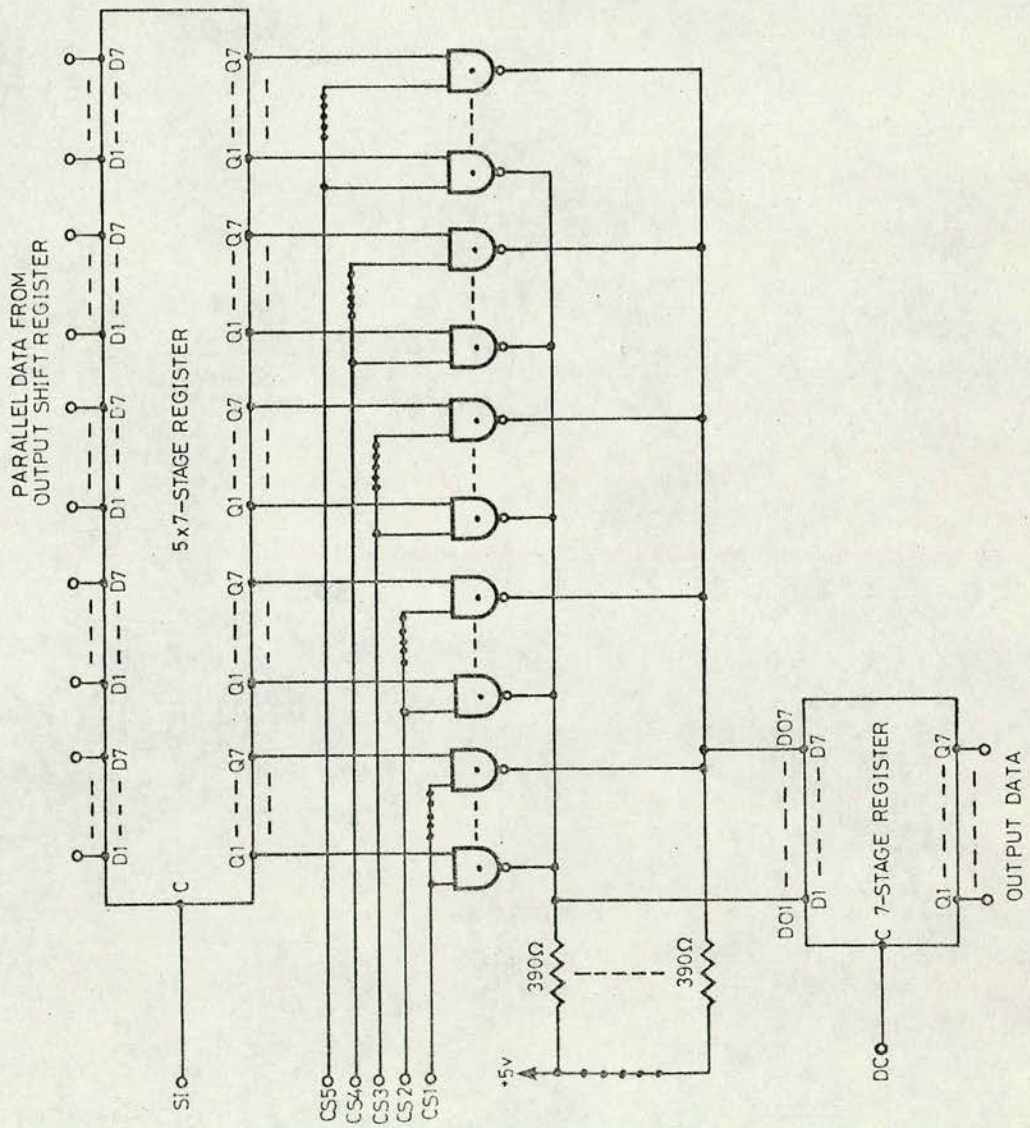


Fig. 4.4.6 Circuit diagram of the output-buffer store and multiplexer.

interest transfers that data to the input of a 7-stage shift register. These data are then stored in the shift register on receipt of the negative-pulse-edge transition of the clock-input control function (denoted here by DC).

Other techniques of multiplexing the various data channels are, of course, available by making use of the frame-synchronisation timing mechanism. In this system, however, the computer (or other processing device) may select and accept data at its own command.

This completes a discussion of the analysis and design of the trial telemetry system. It remains, now, to investigate the performance of the system.

CHAPTER 5

EXPERIMENTAL EVALUATION OF THE TRIAL TELEMETRY SYSTEM

5.1 General

The choice and design of a prototype digital bio-telemetry system has been considered in detail in the previous chapters. In order to assess the performance of this telemetry system, however, it must be investigated experimentally.

In particular, the experimental work to be described in this chapter investigates four topics, viz.

(i) the transmission characteristics of the TDM/PCM system,

(ii) the i.f. filter transient response to a continuous-wave binary FSK input signal,

(iii) the receiver error-probability/error-rate performance, and

(iv) the noise performance of the receiver frame synchronisation process.

These topics represent the major points of issue in the selection and design of the present system and are considered in turn.

5.2 The transmission characteristics of the trial TDM/PCM system

A detailed analysis of the implementation of the prototype TDM/PCM system has been given in chapter 3. According to this analysis the system operations can be summarised as

(i) the sampling of five data-input channels at a frequency $f_s \approx 1.66$ KHz,

(ii)/

(ii) the quantising and encoding of these samples (A/D conversion) into 7-bit binary code words by a process of successive approximation,

(iii) the further encoding of these 7-bit binary code words into 14-bit balanced code words, and

(iv) the serial output of these five 14-bit data words together with an extra 14-bit code word for receiver synchronisation purposes.

The quality of the TDM/PCM system information transmission capability is directly dependent on the initial sampling and A/D conversion processes. Since these processes occur in sequence and their individual actions are not readily isolated, it is expedient to examine their combined actions. Specifically, the TDM/PCM output characteristics examined are

(i) the overall linearity in sampling and quantising a continuous-wave signal, and

(ii) the variations in quantisation-step heights.

The system arranged for investigating the linearity of the TDM/PCM sampling and quantising processes is illustrated in fig. 5.2.1. An oscilloscope time-base ramp signal (with a specified [72] non-linearity of less than $\pm$ 1 per cent) is used as the test signal. The oscilloscope is interfaced with the TDM/PCM system via a resistive attenuator which ensures

(i) that the maximum voltage level of the test signal just saturates (overloads) the TDM/PCM system input stage, and

(ii)/

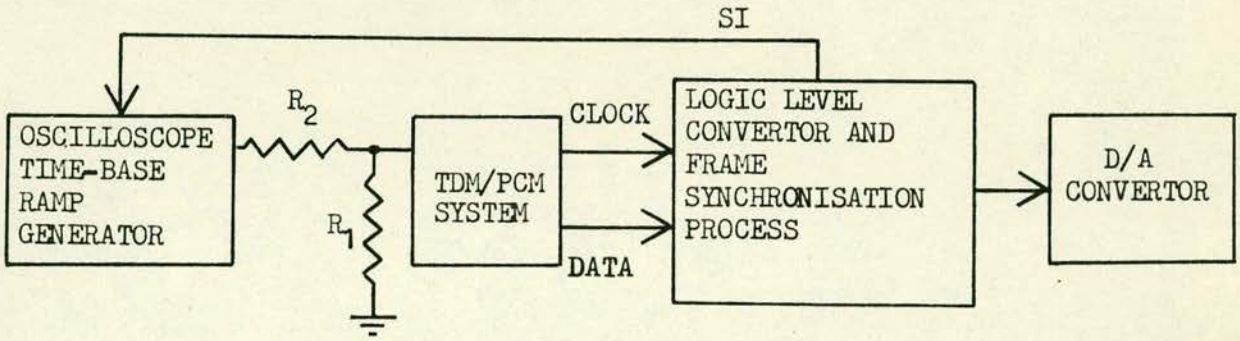


FIG. 5.2.1 System block diagram for testing the linearity of the TDM/PCM sampling and quantising processes.

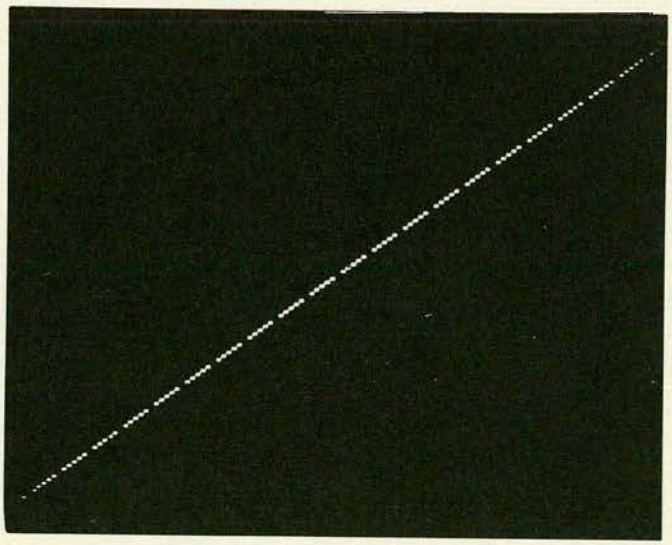


FIG. 5.2.2 Oscilloscope trace of the D/A convertor output for a ramp test signal with critical slope ($3V_s/64T_c$) applied simultaneously to the five data inputs of the TDM/PCM system.

(ii) that the output impedance of the interface [$= R_1R_2/(R_1 + R_2)$] is less than 1KΩ (cf. sect. 3.4 above).

The receiver frame-synchronisation process (described in sect. 4.4 above) is utilised in order to isolate the serial-data output for each channel of the TDM/PCM system. The decoded data for each channel are reconstructed in turn by a D/A convertor at the output of the frame-synchronisation circuit. Continuous monitoring of the D/A convertor output on the oscilloscope screen is made possible by triggering the oscilloscope time-base externally with a signal derived from the frame-synchronisation circuit. [In practice, the logic function SI is used. Sect. 4.4 above refers.]

The oscilloscope trace of fig. 5.2.2 illustrates the D/A convertor output with the ramp test-input signal applied simultaneously to the five data-inputs of the trial TDM/PCM system. If V_s represents the dynamic range of the PCM encoder (cf. subsection 3.3.3 above) and T_c $(= 1/f_s)$ represents the channel sampling period of the TDM system, the slope s_r of the ramp input signal is chosen to be

$$s_r = 3V_s/64\ T_c \qquad .....(5.2.1)$$

$$= 6\sigma/T_c \qquad .....(5.2.2),$$

where $\sigma\ (\equiv V_s/128)$ is the quantisation-step height. It can be seen that the D/A convertor output increases continuously at the desired rate of one quantisation-step per channel data word until the ramp-input signal overloads the PCM encoder. [The occurrence of zero volts at every sixth step indicates the decoding of the frame-synchronisation data words.] The overall linearity of the TDM/PCM/

TDM/PCM system sampling and quantising processes is thus verified experimentally.

In order to investigate the variations between quantisation-step heights, on the other hand, the ramp generator utilised in the test system described above is replaced by a variable voltage source and a digital voltmeter. Accurately measured test input voltage levels are applied simultaneously to the five data inputs of the TDM/PCM system and the corresponding response of each transmitted data channel is monitored at the D/A convertor output. Two significant results were observed, viz.

(i) that the variation in the measured quantisation-step heights for the individual channels is within five per cent (and therefore meets the design specifications discussed in subsection 3.3.3 above), and

(ii) that, between channels, there is a small variation in the level of each quantisation step, these variations being found to be within ten per cent of the desired step height.*

[The second type of variation could be troublesome in supercommutated systems in which one information signal feeds more than one data input.]

Except for the variation in step height between different channels, the experimental investigation has shown that the quality of the TDM/PCM system information transmission capability meets the standard specified by the design criteria discussed in chapter 3. Such a variation between channels was not anticipated but, in view of the amount of variation (viz. ten per cent of the desired step height), it might reasonably be assumed to have an insignificant effect in the present system.

* This is equivalent to a d.c. offset of 0.1 per cent of the dynamic range.

5.3 The i.f. filter transient response to a binary-FSK input signal

The bandwidth requirements of several band-pass filters, for use with both discriminator detection and 'dual-filter' envelope detection of a continuous-wave binary FSK signal, have been derived theoretically (in sect. 2.6 above). As these results lead eventually to the selection of discriminator detection for the telemetry system being investigated, their validity is examined here with respect to the filter implemented in the present receiver system (viz. the critically-coupled tuned band-pass filter).

The bandwidth requirements for discriminator detection filter systems were obtained by examining two components in the filter response to a simulated continuous-wave binary-FSK signal, viz.

(i) the envelope response function, and

(ii) the time derivative of the excess-phase response function.

[Sect. 2.6 above refers.] These two response functions are therefore investigated experimentally.

A block diagram of the experimental system is given in fig. 5.3.1. An FSK test signal is obtained by using the signal output of a square-wave generator as the control-input signal to a 27-MHz voltage-controlled oscillator. In order to investigate the transient responses of interest, however, the square-wave amplitude is varied to give the desired FSK frequency separation of 125KHz (cf. subsection 4.2.1 above). Moreover, the square-wave frequency is chosen to give an effective bit-period of 20μs, this value being significantly greater than the bit period (viz. 10μs) for which the receiver filter is designed.

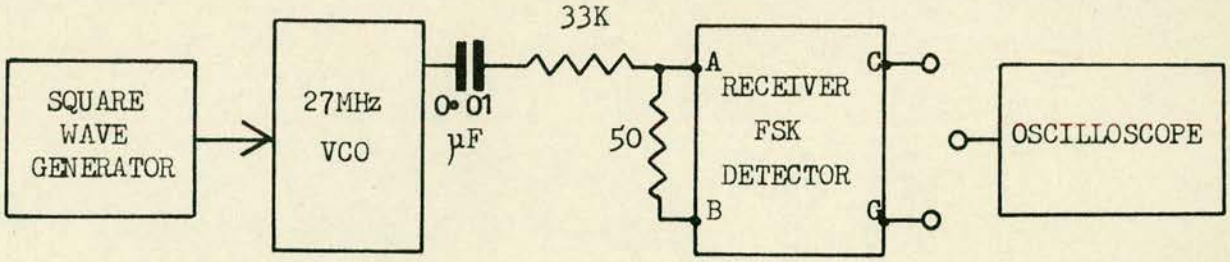


FIG. 5.3.1 System block diagram for examining the i.f. filter bandwidth requirements.

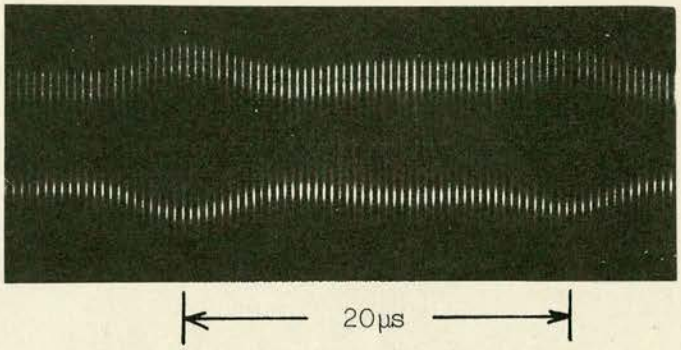


FIG. 5.3.2 Oscilloscope trace of the i.f. filter output to the FSK test signal with bit period 20 μs.

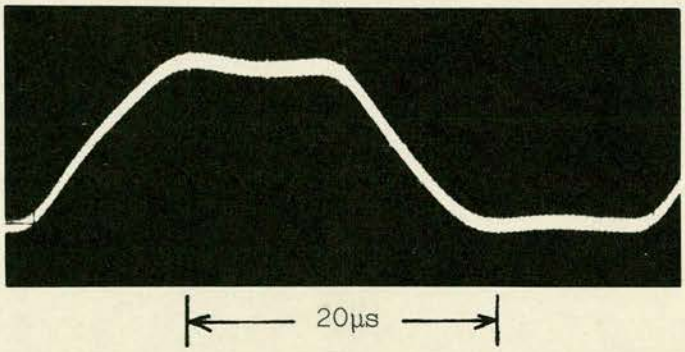


FIG. 5.3.3 Oscilloscope trace of the PLL discriminator response to the FSK test signal with bit period 20 μs.

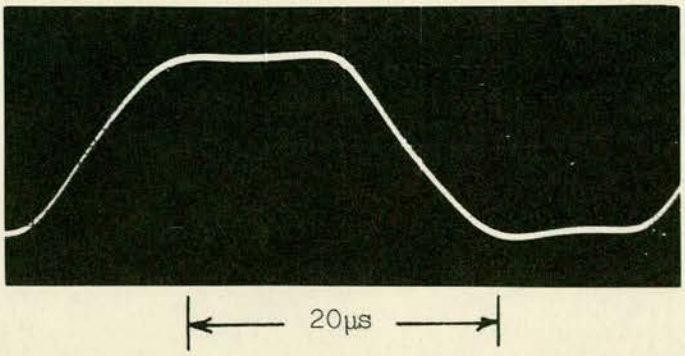


FIG. 5.3.4 Oscilloscope trace of the post-detector filter response to the FSK test signal with period 20 μs.

The FSK test signal thus specified is applied to the mixer input terminals A and B of the FSK detector (cf. fig. 4.2.2 above) through a resistive attenuator. The desired response signals are then obtained by monitoring the FSK detector terminals C and G. [As shown in fig. 4.2.3, terminal C is a single-ended low-impedance output of the i.f. amplifier whilst terminal G is the single-ended output of the phase-locked-loop demodulator.]

The oscilloscope trace of fig. 5.3.2 illustrates the i.f. filter response to a test FSK signal with a bit period of 20μs. Of particular interest is the envelope response function which appears as the amplitude profile of the high-frequency sinusoidal component in the filter response.

The PLLD response to the same FSK test signal is illustrated by the oscilloscope trace of fig. 5.3.3. This signal is essentially the desired time derivative of the filter excess-phase response function together with the low-pass filtering effect of the PLLD transfer function. In accordance with the discussion in sect. 2.3, however, the PLLD transfer function has been designed so that there is virtually no filtering of the desired response function (cf. subsection 4.2.2 above).

The need for a post-detection filter is made manifest by the level of high-frequency harmonic distortion superimposed on the PLLD output signal. One stage of simple RC low-pass post-detection filtering has been implemented (cf. subsection 4.2.3 above) in the FSK detector after terminal G accordingly. The post-detection filter output signal for the same FSK test signal is illustrated/

illustrated by the oscilloscope trace of fig. 5.3.4. In comparison with the PLLD output, it can be seen that the level of distortion is significantly reduced with virtually no additional shaping of the desired response function.

A comparison of the experimental response functions of figs. 5.3.2 and 5.3.3 with the corresponding theoretical response functions of fig. 2.6.1 reveals no significant differences. The bandwidth requirement of this discriminator detection filter system is thus verified. Moreover, the close similarity between the theoretical and practical waveforms tends to substantiate the theoretical waveforms derived for the other filter systems considered (cf. sect. 2.6 above).

5.4 The receiver error-probability performance

In chapter 2, the choice of receiver FSK detection technique is made after consideration of the systems most suitable in this application (viz. 'dual-filter' envelope detection and discriminator detection). Specifically, discriminator detection is chosen since its error-reduction performance is expected to be best for the range of signal-to-noise ratio associated with practical information retrieval. In order to justify this choice, the error-probability of the discriminator detection system implemented is investigated experimentally.

A circuit/block diagram of the experimental system is given in fig. 5.4.1. An FSK test signal is obtained (as in the previous experiment) by allowing a square-wave signal to frequency modulate a 27-MHz voltage-controlled oscillator. The square-wave amplitude is/

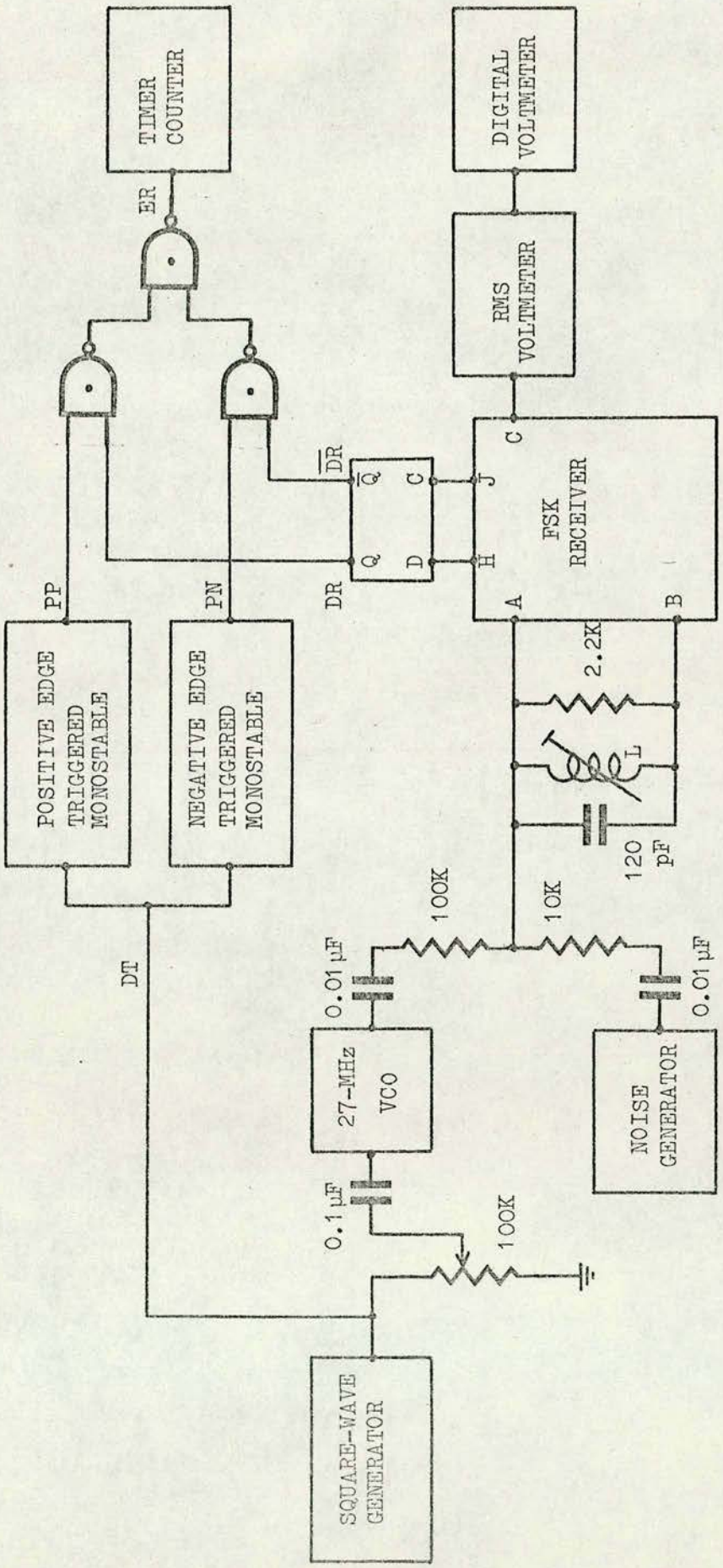


Fig. 5.4.1 A circuit/block diagram of the experimental system to determine the receiver probability of error characteristic.

is set to give the optimum FSK frequency separation of 125KHz for the present i.f. filter (cf. subsection 4.2.1 above), whilst the square-wave frequency is set to give the desired bit period of 10μs (cf. subsection 3.3.1 above). Together with the output signal of a Gaussian noise generator, the FSK test signal is applied to the mixer input terminals A and B of the FSK receiver system (cf. fig. 4.2.2 above). [The design of the noise generator is described in appendix 7 below.] A broad-band tuned filter at the same terminals simulates the effect of r.f. filtering and also restricts the Gaussian noise spectrum to the reception band of specific interest. The received-bit pattern (denoted here by DR) is constructed by clocking the squared FSK detector output signal from receiver terminal H (cf. fig. 4.2.4 above) into a D-type flip-flop, the clock-input function being the regenerated clock appearing at receiver terminal J (cf. fig. 4.3.1 above).

For error detection, the received-bit pattern is compared with the transmitted-bit pattern. It should be noted that, in comparison with the transmitted-bit pattern, the regenerated-bit pattern is delayed in time (by approximately half a bit-period). This feature, together with the fact that the transmitted-bit pattern is a combination of alternate '1' and '0' bits, makes the error-detection system relatively simple.

Specifically, the transmitted-bit pattern (denoted here by DT) is used to define two test patterns of short duration pulses (the pulse 'on' periods being less than 1μs). One test pattern

PP/

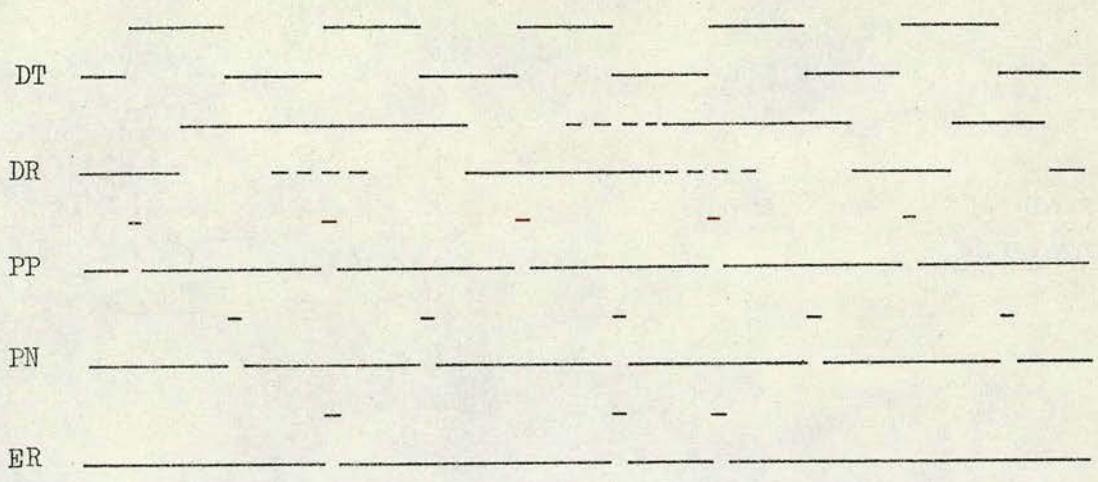
PP (say) is obtained from a positive-edge-triggered monostable, whilst the other pattern PN (say) is obtained from a negative-edge-triggered monostable (cf. fig. 5.4.1). In view of the time displacements between the transmitted- and received-bit patterns, the functions PP and PN are then used to test for errors in transmitted '0' and '1' bits respectively. The error function ER is given by

$$ER = PP.DR + PN.\overline{DR} \qquad .....(5.4.1).$$

A timing diagram of these various functions is given in fig. 5.4.2, the function ER being defined for a hypothetical error condition in DR as shown.

The error-rate f_e (i.e. the total number of errors per second) is found in this system by taking the output function ER to a timer counter which then counts the error pulses in a given time period. Since the transmitted bit-rate f_b is known accurately (viz. 100KHz), the error probability P_e for a given noise level in the receiver i.f. filter is obtained experimentally as the ratio f_e/f_b.

Noise measurements in the receiver i.f. system are made at the i.f. amplifier output terminal C (cf. fig. 4.2.2 above) with the aid of a true-r.m.s. wide-band voltmeter and a d.c. digital voltmeter. In particular, measurement accuracy is increased by taking the output signal of the r.m.s. meter to the digital voltmeter. The output of the digital voltmeter represents the measured r.m.s.-value scaled by a constant factor. Evaluation of this scale factor is not necessary, however, since the desired experimental values are obtained as ratios of carrier power to noise power.



--- indicates the existence of errors in the received data

Fig. 5.4.2 Timing diagram of the error-detection waveforms.

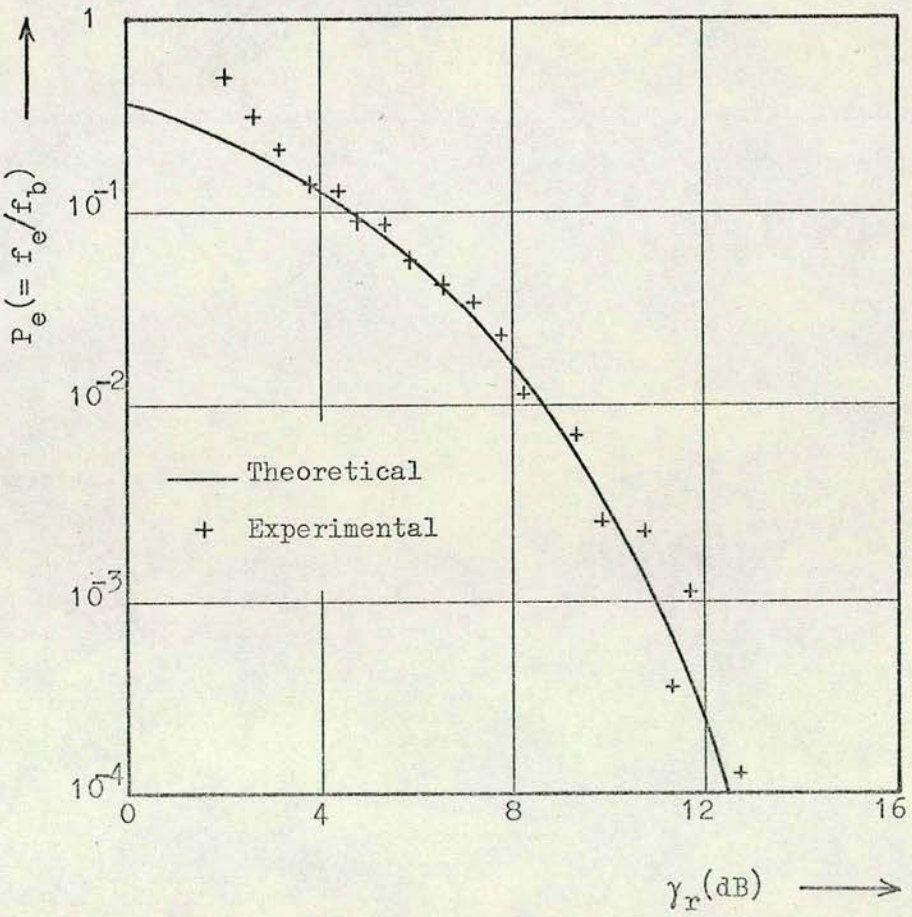


Fig. 5.4.3 Error probability characteristic for discriminator detection with a critically-coupled tuned filter.

With the noise generator and square-wave generator switched 'out of circuit', the r.m.s.-carrier amplitude $\bar{A}_r$ is measured. With the noise generator switched 'in circuit', the r.m.s. amplitude $\bar{A}_{r+n}$ is measured. Accordingly, the r.m.s. noise amplitude $\bar{A}_n$ at the i.f. filter output can be found from [10, 11, 12]

$$(\bar{A}_n)^2 = (\bar{A}_{r+n})^2 - (\bar{A}_r)^2 \qquad \ldots\ldots(5.4.2),$$

and the i.f. carrier-to-noise power ratio γ_r is then obtained from

$$\gamma_r = (\bar{A}_r)^2/(\bar{A}_n)^2 \qquad \ldots\ldots(5.4.3).$$

The corresponding value of error-rate is obtained with the square-wave generator switched 'in circuit'.

The error-probability characteristic thus obtained is given in fig. 5.4.3 together with a plot of the theoretical characteristic for the present discriminator detection system (as derived in sect. 2.5). It can be seen that there is excellent agreement between the theoretical and experimental results for values of γ_r in the range 4 to 10 dB.

For values of γ_r larger than 10 dB, however, the experimental points are not so closely grouped about the theoretical curve. This is due to the fact that, for large values of signal-to-noise ratio, the noise power becomes progressively smaller and more difficult to measure accurately. [Equation (4.5.2) refers.] The experimental error in measuring γ_r increases accordingly.

For values of γ_r below 4dB, on the other hand, the experimental data diverge from the theoretical curve. In particular, the measured experimental values of error probability are larger than the theoretical values. Since the experimental error in measuring γ_r is very small in this range, the divergence must be taken as characteristic of the practical system.

An increase in the value of error probability at low values of received signal-to-noise ratio is to be expected in practical systems for two reasons, viz.

(i) the operation of the circuit to provide the phase-coherent receiver-based clock becomes progressively more unstable (cf. sect. 4.3 above), and

(ii) the performance of the phase-locked-loop discriminator is reduced for input signal-to-noise ratios which fall below its particular threshold value (cf. sect. 2.3 above).

In the present design, the clock regeneration circuit is found to be stable for $\gamma_r > 2$dB. Accordingly, we conclude that $\gamma_r = 4$dB corresponds to the threshold value of signal-to-noise ratio associated with the PLLD. This value corresponds to the value of PLLD threshold level derived by Gagliardi[44].

From this analysis of the experimental results, we see that no unexpected effects are obtained. Indeed, there is excellent agreement between the theoretical and experimental values for error probability, thus justifying the choice of discriminator detection as the FSK reception technique.

5.5 The noise performance of the receiver frame-synchronisation process

Referring to the discussion in sect. 4.4, the specification of a minimum received-signal strength is facilitated by experimental evidence that the receiver frame-synchronisation process is not significantly effected by Gaussian noise effects provided the received signal-to-noise ratio is above a certain value. The relevant experimental study is described in this section.

A circuit/block diagram of the experimental system is given in fig. 5.5.1. The test FSK signal is obtained by allowing the output of the prototype TDM/PCM transmitter system to modulate a 27-MHz carrier, taking care (as described in the previous two sections) that the amplitude of the modulating waveform defines the optimum frequency separation (=125KHz) for this FSK receiver system. The interface circuitry between the 27-MHz voltage-controlled oscillator, the Gaussian-noise generator, and the input to the FSK receiver is the same as that described in the previous section and is not therefore discussed here.

The procedure for investigating the TDM/PCM system (cf. sect. 5.2 above) is used again here, since it facilitates the continuous monitoring of the recovered test signal at the output of the D/A convertor.

Noise measurements are made at the receiver i.f. amplifier output terminal C (cf. fig. 4.2.2 above) according to the technique described in the previous section.

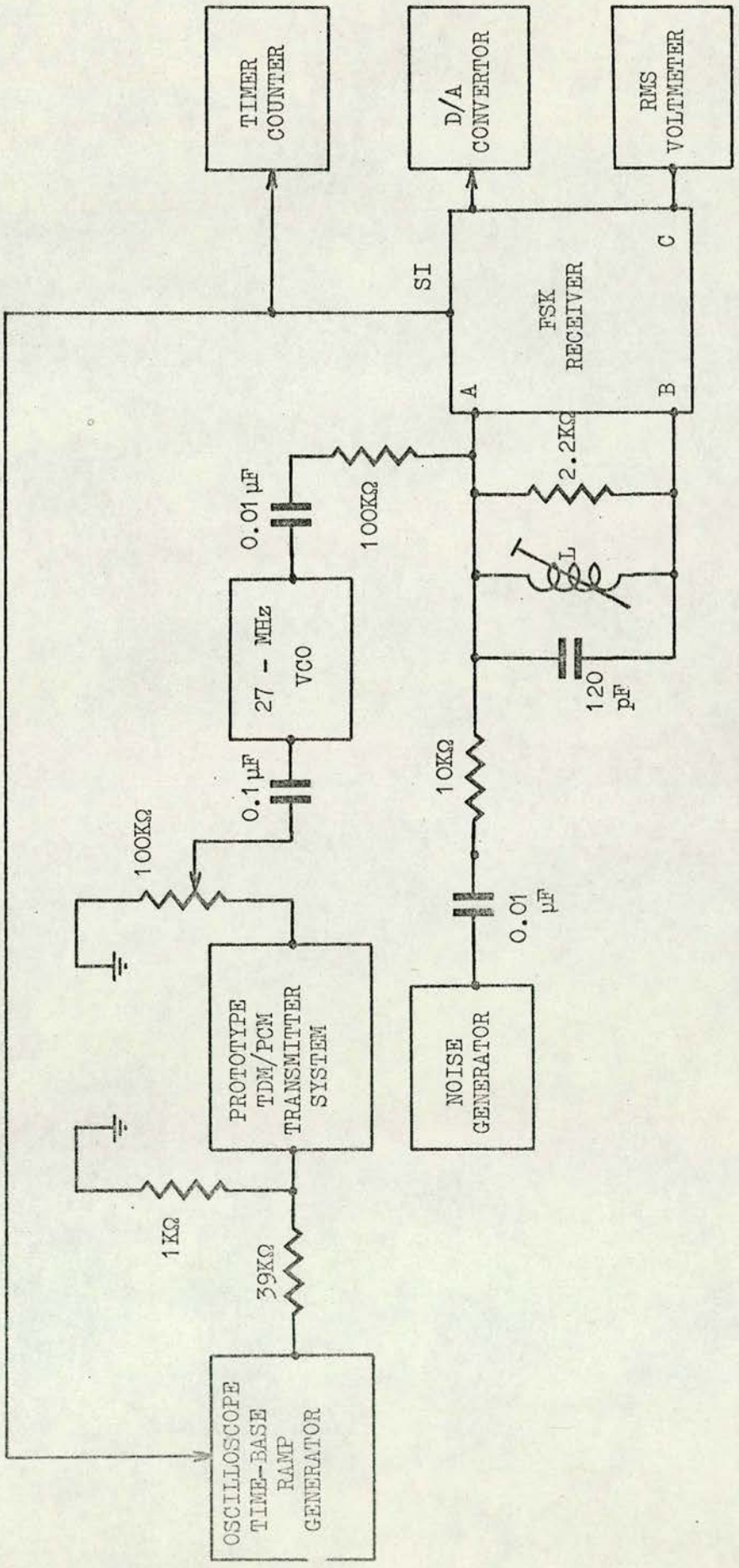


Fig. 5.5.1 A circuit/block diagram of the experimental system to find the noise performance characteristic of the receiver frame-synchronisation process.

In practice, the recovery of a discrete frame of information is indicated in the receiver by the generation of a pulse denoted by the logic function SI. [Fig. 4.4.2 refers.] Accordingly, a measure of the effect of a particular noise level on the performance of the receiver frame-synchronisation process is found from the pulse rate f_p (say) associated with the logic function SI. Although there is some finite probability that each pulse may define a false synchronisation condition, it is impracticable to distinguish between this state and true synchronisation; no attempt is made to distinguish between correct and incorrect pulses accordingly.

Since the normal pulse-rate associated with the logic function SI will be the same as the system channel-sampling frequency $f_s (= f_b/84)$, it is convenient to show the effect of Gaussian noise on the frame-synchronisation process by plotting the ratio f_p/f_s as a function of the signal-to-noise ratio γ_r obtained at the i.f. amplifier output. The curve obtained for the present system is shown in fig. 5.5.2. It can be seen to have two significant features:-

(i) For $\gamma_r > 7$dB, the effect of Gaussian noise causes virtually no loss of frame synchronisation. [It should be noted, however, that there is always some finite probability (albeit small for $\gamma_r > 7$dB) that frame synchronisation can be lost due to Gaussian noise effects.]

(ii) For $\gamma_r < 4$dB, there is a reduction in the rate of decrease of the measured value of f_b. Since this characteristic occurs at low values of γ_r and therefore at high error rates, the implication is that false synchronisation decisions are made and/

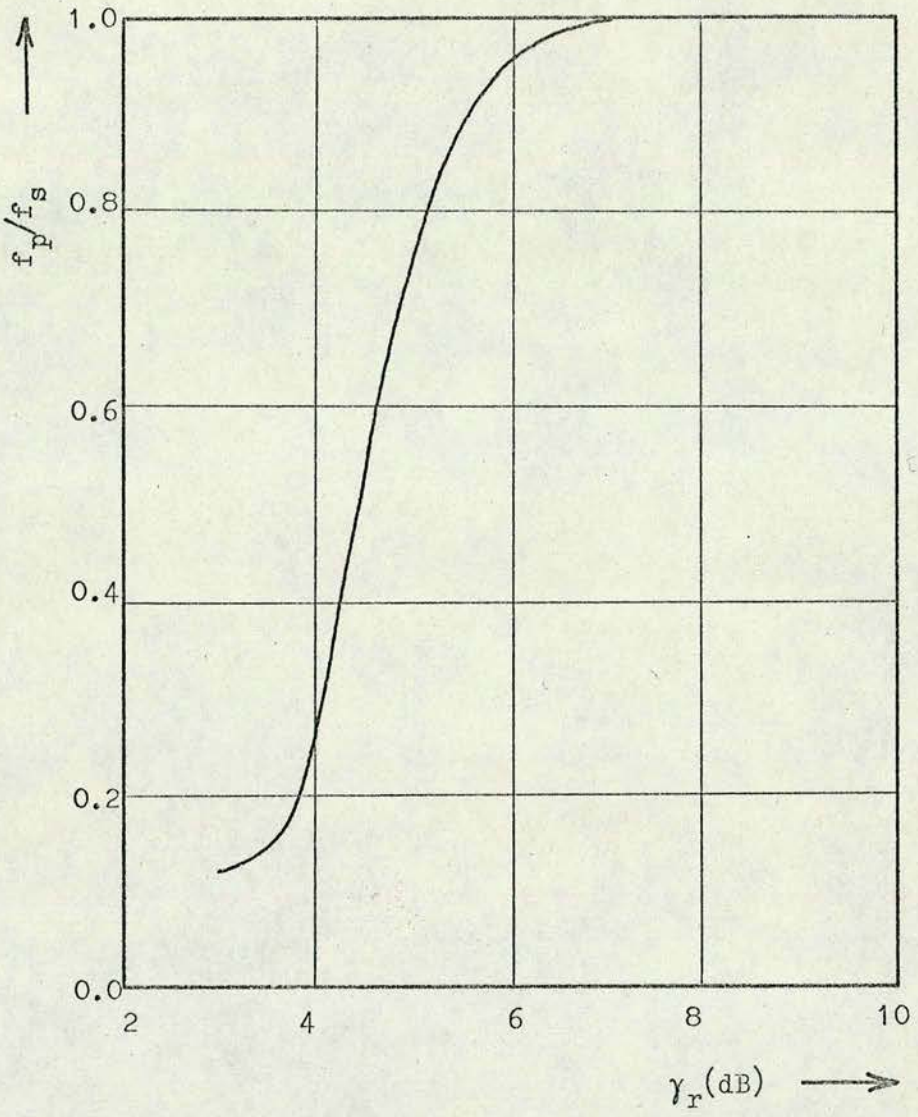


Fig. 5.5.2 Curve of f_p/f_s vs. γ_r for the receiver frame-synchronisation process.

FILTER TYPE*	CCT	BF3	BF4	BF5	BF6
THRESHOLD VALUE OF γ_r(dB)	7	6.4	6.0	5.9	5.8

Table 5.5.1

* BFk denotes Bessel filter of order k
CCT denotes critically-coupled tuned filter

and retained at an increasing rate. In the present system, however, this feature is of no practical importance. Accordingly, it is not considered further.

From (i) above, it is apparent that γ_r = 7dB is essentially a threshold level below which useful data retrieval with the present receiver system is not possible. The operational threshold of the receiver frame-synchronisation process, however, is more suitably defined with respect to error-rate or error-probability, its performance being directly related to errors in the recovered bit pattern. For the present system, the error-probability threshold is deemed to be 0.04, the value of error-probability corresponding to γ_r = 7dB (cf. fig. 5.4.3 above).

Since different receiver filter systems may produce different error rates for the same basic transmission parameters (cf. sect. 2.5 above), the threshold level of γ_r is filter dependent. The error-probability threshold, on the other hand, describes the operational capability of only the receiver frame-synchronisation process and is therefore independent of filter type. Accordingly, it may be utilised to determine the threshold values of γ_r associated with other possible receiver filter systems, the relevant values of γ_r being specified with respect to the error probability value of 0.04. For example, the threshold values of γ_r corresponding to the range of filter systems examined in chapter 2 are listed in table 5.5.1.

The foregoing experimental results are best substantiated by illustrating the features of data recovery for reception conditions existing above and below the threshold level. [The test arrangement of/

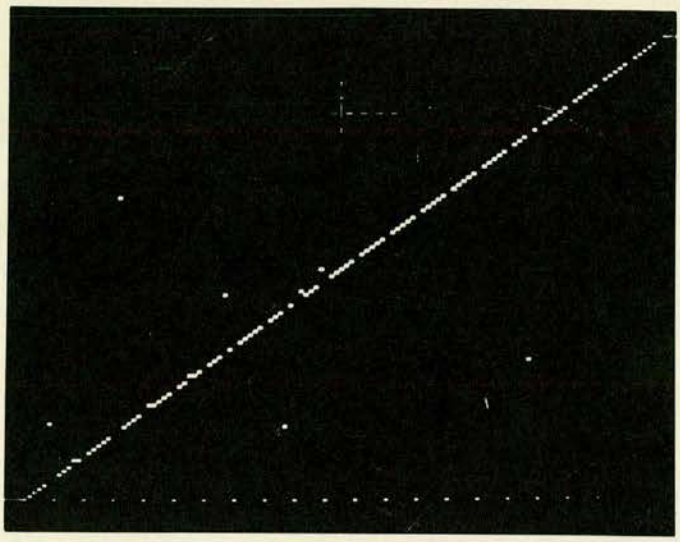


FIG. 5.5.3 Oscilloscope trace showing the effect of noise on the recovered ramp test signal for $\gamma_r \approx 9$dB.

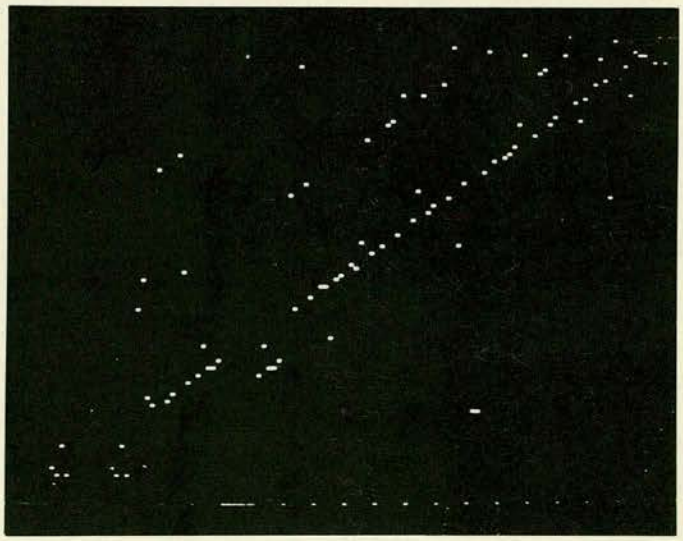


FIG. 5.5.4 Oscilloscope trace showing the effect of noise on the recovered ramp test signal for $\gamma_r \approx 5$dB.

of fig. 5.5.1 facilitates the continuous monitoring of the recovered ramp test signal which is corrupted by Gaussian noise during transmission.] Accordingly, the recovery of the ramp test signal is illustrated in figs. 5.5.3 and 5.5.4 for $\gamma_r \approx 9$dB and $\gamma_r \approx 5$dB respectively (these values of γ_r being respectively larger and smaller than the threshold value of 7dB specified for the present system).

For $\gamma_r \approx 9$dB, it can be seen that there is no loss of frame synchronisation and only sporadic decoding errors appear in the recovered data. For $\gamma_r \approx 5$dB, on the other hand, the recovered data are badly corrupted by a great number of decoding errors and also by the loss of frame synchronisation. [The loss of frame synchronisation is indicated in the oscilloscope trace of fig. 5.5.4 by the recovered signal assuming the value of zero volts along with the frame synchronisation word data.]

This concludes the experimental analysis of the present trial telemetry system.

C O N C L U S I O N

In chapter one, a multi-channel TDM/PCM continuous-wave FSK system was shown to provide the digital-telemetry technique most suitable for the low-power, near-field radio transmission of several channels of biological data from an implanted source. A prototype system has been investigated (in chapters 2 to 5 inclusive) in order to assess the operational characteristics of this telemetry technique, an essential precursor to the costly design and fabrication of a hybrid LSI/thin-film micro-circuit suitable for implantation as the transmitter source. The five items considered to be of major importance in such an assessment are discussed briefly here:-

(i) The original concept of utilising COS/MOS digital techniques[8] in a TDM/PCM system has been substantiated practically by examining the transmission characteristics of the trial system fabricated using commercially available MSI devices (cf. sect. 5.2 above). Since the discrete medium-scale-integrated COS/MOS devices interface directly, no problems are therefore anticipated in the design and fabrication[73] of a corresponding large-scale-integrated device necessary for implantation.

(ii) As demonstrated in chapter 3, the prototype TDM/PCM system is designed with the special requirements of an implantable system very much in mind. Of particular significance in this objective is the implementation of a successive approximation A/D convertor which allows simpler analogue circuitry (the basic requirement for all thin-film implantable systems[5]). Notably, the prototype system allows for a transducer output impedance level of up to 1KΩ (cf. sect. 3.4 above) and, moreover,/

moreover, avoids the use of a buffer stage between the system D/A convertor and comparator circuits (cf. sect. 3.3 above). The performance of the prototype TDM/PCM system incorporating these design features has been verified experimentally (cf. sect. 5.2 above).

(iii) The major problem of any telemetry system with an implanted source is in coping with a slow reduction in power supply voltage as the power cells discharge, the implementation of extra voltage-controlling circuitry being undesirable from the point of view of implantation. In the prototype digital-telemetry system, two major effects are observed due to a variation in supply voltage, viz.

(a) the dynamic range of the system A/D convertor changes in direct proportion (cf. subsection 3.3.3 above), and

(b) the r.f. carrier frequency drifts (cf. sect. 3.6 above).

To cope with effect (a), a receiver-based reference signal, obtained by monitoring the transmitter power supply voltage, could be used to make compensatory adjustments. From the point of view of implantation, the proposed digital telemetry system is particularly suitable for the inclusion of such an extra data channel since it would effectively require only a simple voltage-monitoring circuit, the extra digital control and sampling circuits being provided on an LSI micro-circuit.

To cope with effect (b), on the other hand, an r.f. tuner incorporating an AFC circuit is implemented in the receiver FSK detector (cf. sect. 4.2 above). The operation of this circuit has been found to be satisfactory for received signal-to-noise ratios as low as 2dB. [This was the lowest value

of/

of signal-to-noise ratio at which the performance of the FSK detector was investigated experimentally (cf. sect. 5.4 above).]

(iv) The selection of discriminator detection as the receiver FSK detection technique for the proposed telemetry system has been justified experimentally. In particular, the results obtained from an experimental determination of

(a) the system i.f. filter transient response functions (cf. sect. 5.3 above), and

(b) the system error-probability characteristic (cf. sect. 5.4 above)

confirm the corresponding theoretical predictions for the discriminator detection technique implemented.

(v) The noise performance of the complete prototype receiver system has also been investigated (cf. sect. 5.5 above). From the results obtained, it is possible to specify a threshold level of received signal-to-noise ratio below which the present system is not capable of useful data retrieval. Practically, this feature implies that the r.f. link should be designed so as to produce a minimum received signal-to-noise ratio which is greater than the threshold level.

In conclusion, the operation of the prototype system demonstrates that the multi-channel digital telemetry system proposed in this thesis is suitable for the low-power, near-field radio transmission of several channels of biological data from an implanted source. The implementation of a practical transmitter source with the special size and power requirements for implantation is made possible with modern micro-electronic techniques.

APPENDIX 1

COMPUTATION OF THE BAND-PASS FILTER PARAMETERS B AND B_s

The band-pass filter parameters of interest (B and B_s) have been defined (in sect. 2.3 above) with respect to the filter attenuation characteristic $\left|H_b(\omega)\right|^2$ and centre frequency ω_c by the formulae

$$B \equiv \frac{1}{2\pi} \int_0^\infty \left|H_b(\omega)\right|^2 d\omega \qquad \text{.....(A1.1)},$$

and

$$B_s \equiv \frac{1}{2\pi} \int_0^\infty \left|H_b(\omega)\right|^2 (\omega - \omega_c)^2 \, d\omega \qquad \text{.....(A1.2)}.$$

The filter transfer function $H_b(\omega)$ may be written [46]

$$H_b(\omega) \equiv \frac{G_b (j\omega)^k}{\prod_{r=1}^{k} (j\omega - \alpha_r)(j\omega - \alpha_r^*)} \qquad \text{.....(A1.3)},$$

where G_b is the filter gain, k is the filter order, and α_r, together with the complex conjugate α_r^*, are roots of the 2k-th order denominator polynomial.

A computer program was developed to expedite the computation [74,75] of expressions (A1.1), (A1.2) and (A1.3) for the filters of interest (as specified in sect. 2.5 above). In particular, the integrals of expressions (A1.1) and (A1.2) are evaluated using the Trapezium Rule [76,77] according to which they may be written respectively as

$$B = \frac{1}{2\pi} \sum_{n=1}^{N} \tfrac{1}{2} \left\{ \left|H_b(\omega_n)\right|^2 + \left|H_b(\omega_{n+1})\right|^2 \right\} \Delta\omega \qquad \text{.....(A1.4)},$$

and/

and

$$B_s = \frac{1}{2\pi} \sum_{n=1}^{N} \frac{1}{2}\left\{\left|H_b(\omega_n)\right|^2(\omega_n - \omega_c)^2 + \left|H_b(\omega_{n+1})\right|^2(\omega_{n+1} - \omega_c)^2\right\}\Delta\omega \quad \text{.....(A1.5)},$$

where N-1 is the number of $\Delta\omega$ steps in the integration range of interest, and ω_n is the frequency value associated with the n-th step.

A statement listing of the program (in Fortran IV language [78]) is given below.

```
C
C
C      DETERMINATION OF FILTER PARAMETERS BY NUMERICAL INTEGRATION
C
C
       IMPLICIT REAL*8(A-H,O-Z)
       DIMENSION WW(2),WX(2)
       COMPLEX*16 CBPRT(20),DEN,CW,NUM
       DATA PI/3.141592653589793/
C
C
  100 FORMAT(I2)
  300 FORMAT(2D22.15)
  400 FORMAT(2F10.7)
  500 FORMAT('1',7X,'F',12X,'WW',11X,'WX',9X,'SUMB0',8X,'SUMB2')
 1000 FORMAT('0',5D13.5)
 1100 FORMAT('0','FC1=',F8.4,':FC2=',F8.4,':BF=',F8.4)
 1300 FORMAT(' ',I2,2D24.15)
 1400 FORMAT('0',2D24.15)
 1600 FORMAT('-','G FACTOR CONSTANT =',D13.5)
 1700 FORMAT(2I4)
C
C
       READ(5,100)MBP
       READ(5,300)GAINBP
       DO 200 J=1,MBP
  200 READ(5,300)CBPRT(J)
       READ(5,400)FC1,FC2
C
C
       WC=(FC2+FC1)*PI
       BW=2.0D0*PI*(FC2-FC1)
       FC=WC/2.0D0/PI
       BF=BW/2.0D0/PI
C
C
       DO 1200 J=1,MBP
 1200 WRITE(6,1300)J,CBPRT(J)
       WRITE(6,1400)GAINBP
       WRITE(6,1100)FC1,FC2,BF
C
C
C      INITIALIZATION OF VARIABLES
C
C
       READ(5,1700)N,NBW
       DW=2*NBW*BW/(N-1)
       W=WC-NBW*BW
       SUMB0=0.0D0
       SUMB2=0.0D0
       WRITE(6,500)
```

```
C
C
      DO 600 J=1,N
      F=W/2.0D0/PI
      CW=DCMPLX(0.0D0,W)
      DEN=(1.0D0,0.0D0)
      DO 700 I=1,MBP
  700 DEN=DEN*(CW-CBPRT(I))
      ARGDEN=CDABS(DEN)
      NUM=GAINBP*CW**(MBP/2)
      ARGNUM=CDABS(NUM)
C
C     WW IS ATTENUATION VALUE
C     WX IS SECOND MOMENT VALUE
C
      WW(1)=(ARGNUM/ARGDEN)**2
      WX(1)=WW(1)*(W-WC)**2
      IF(J.EQ.1) GO TO 900
C
C     TRAPEZIUM RULE INTEGRATION OF WW AND WX
C
      SUMB0=SUMB0+((WW(1)+WW(2))*DW/2.0D0)/2.0D0/PI
      SUMB2=SUMB2+((WX(1)+WX(2))*DW/2.0D0)/2.0D0/PI
      IF(JJ*2*100/(N-1).NE.1) GO TO 1500
C
  900 WRITE(6,1000)F,WW(1),WX(1),SUMB0,SUMB2
      JJ=0
 1500 WW(2)=WW(1)
      WX(2)=WX(1)
      JJ=JJ+1
  600 W=W+DW
C
C
      FACTOR=DSQRT(SUMB0/SUMB2)
      WRITE(6,1600)FACTOR
      STOP
      END
```

APPENDIX 2

COMPUTATION OF THE BAND-PASS FILTER RESPONSE FUNCTIONS

In sect. 2.6 above, the band-pass filter response $v_o(t)$ was derived for a binary FSK input signal. The expression obtained for $v_o(t)$ may be written in the form

$$v_o(t) = e_o(t) \cos\left\{\omega_2(t - t_c) + \theta_{j2} + \phi_o(t)\right\} \qquad \ldots\ldots(A2.1),$$

in which the functions $e_o(t)$ and $\phi_o(t)$ (representing the envelope and excess-phase response functions respectively), together with $\dot{\phi}_o(t)$, are of particular interest.

The expressions obtained for $e_o(t)$, $\phi_o(t)$ and $\dot{\phi}_o(t)$ are extremely complicated (cf. sect. 2.6 above). [They are not therefore reproduced here.] Accordingly, a computer program was developed to expedite the computation of these response functions for the range of filters and corresponding filter input signals of interest (as specified in sect. 2.6 above).

A statement listing of the program (in Fortran IV language [78]) is given below.

```
C
C
C      BP FILTER RESPONSE BY THE METHOD OF RESIDUES
C
       IMPLICIT REAL*8(A-H,O-Z)
       COMPLEX*16 CLPRT(10),ARG(10),CBPRT(22),DEN,LOP,NUMC,NUMS,
      /DLPRT(10),CCL(22),CSL(22),CCH(22),CSH(22),RESP2,RESP3,SUMVR2,
      /SRCL,SRSL,SRCH,SRSH,VAR,VO,CFACT,CHECK(20),SRCLT
       COMPLEX*16 LFR(22),HFR(22)
       DIMENSION ISW(7)
       DIMENSION CL(2,22),SL(2,22),CH(2,22),SH(2,22)
       DIMENSION RL(2,22),RH(2,22)
       DIMENSION AMPCL(11),AMPSL(11),PHICL(11),PHISL(11)
       DIMENSION AMPCH(11),AMPSH(11),PHICH(11),PHISH(11)
       DIMENSION ALPHL(11),ALPHH(11),BETAL(11),BETAH(11)
       EQUIVALENCE (CCL(1),CL(1,1)),(CSL(1),SL(1,1))
       EQUIVALENCE (CCH(1),CH(1,1)),(CSH(1),SH(1,1))
       EQUIVALENCE (LFR(1),RL(1,1)),(HFR(1),RH(1,1))
       LOGICAL LA,LC
       DATA PI/3.141592653589793/
       DATA IYES/'YES'/
    10 FORMAT(I2,1X,I2)
    30 FORMAT(2D22.15)
    40 FORMAT(4F10.7,2D14.7)
    50 FORMAT(4D14.7)
    60 FORMAT('-',' J','  CLPRT'/)
    80 FORMAT(' ',I2,2D24.15)
    90 FORMAT('-',' J','  VALUE OF CLPRT AFTER TRANSFORMATION FACTOR'/
   110 FORMAT('-',' J','  CBPRT=(CLPRT+SQRT)/2'/)
   130 FORMAT(' ',I2,2D24.15,12X,2D24.15/' ',62X,2D24.15)
   190 FORMAT('1',' J',3X,'CCL',28X,'CSL',28X,'CCH',28X,'CSH')
   210 FORMAT(' ',I2,4(1X,2D15.7))
   220 FORMAT('1','TIME RESPONSE OF VO'/)
   290 FORMAT(' ',D13.7,5(D15.4,F8.4))
   310 FORMAT('-',' LOP=',2D24.15,': DEN=',2D24.15/)
   320 FORMAT(' ','CFACT=',2D24.15,': DEN=',2D24.15)
   330 FORMAT('-',' J','  CHECK'/)
   350 FORMAT('0','FC1=',F8.4,':FC2=',F8.4,':F1=',F8.4,':F2=',F8.4)
   360 FORMAT('0',4F10.4,2D16.7)
   370 FORMAT('0',4D16.7)
   380 FORMAT('0','GAINBP=',D24.15)
   404 FORMAT('-',' J',3X,'CLFRTS',25X,'CHFRTS')
   500 FORMAT(5F13.7)
   501 FORMAT('-','IL=',I2,':IH=',I2)
   502 FORMAT('-',4X,'AMPCL',8X,'AMPSL',8X,'ALPHL',
      /           8X,'BETAL',8X,'PHICL',8X,'PHISL')
   504 FORMAT(' ',6F13.7)
   505 FORMAT('-',4X,'AMPCH',8X,'AMPSH',8X,'ALPHH',
      /           8X,'BETAH',8X,'PHICH',8X,'PHISH')
   507 FORMAT('-','W1=',F13.7,':W2=',F13.7)
   342 FORMAT('-',' RESET VALUES OF CBPRTS')
   344 FORMAT('0',2D14.7)
```

```
352 FORMAT('0','RESET GAINBP =',D14.7)
670 WRITE(6,720)
720 FORMAT(' WHICH DATA GROUPS?')
    READ(5,721)ISW
721 FORMAT(711)
    DO 800 I=1,7
    ISWU=ISW(I)+1
    GO TO (800,801,802,803,804,805,806,807),ISWU
801 WRITE(6,700)
700 FORMAT(' IPASS,NPASS? ')
    READ,IPASS,NPASS
     GO TO 800
802 WRITE(6,701)
701 FORMAT(' MLP? ')
    READ,MLP
    MBP=2*MLP
    GO TO 800
803 WRITE(6,702)
702 FORMAT(' CLPRT, MLP TIMES? ')
    DO 730 J=1,MLP
    READ,DLPRT(J)
730 CONTINUE
    GO TO 800
804 WRITE(6,703)
703 FORMAT(' FC1,FC2,F1,F2? ')
    READ,FC1,FC2,F1,F2
    GO TO 800
805 WRITE(6,704)
704 FORMAT(' PTS1,PTS2,WTS1,WTS2,DELAY1,DELAY2? ')
    READ,PTS1,PTS2,WTS1,WTS2,DELAY1,DELAY2
    GO TO 800
806 WRITE(6,705)
705 FORMAT(' TAW1,TAW2,TIME,DELAY3,DELT? ')
    READ,TAW1,TAW2,TIME,DELAY3,DELT
    GO TO 800
807 WRITE(6,706)
706 FORMAT(' CNORM,CSTLP? ')
    READ,CNORM,CSTLP
800 CONTINUE
    IO=10
    WRITE(IO,350)FC1,FC2,F1,F2
    WRITE(IO,360)PTS1,PTS2,WTS1,WTS2,DELAY1,DELAY2
    WRITE(IO,370)TAW1,TAW2,TIME,DELAY3
    WRITE(IO,370)CNORM
    WRITE(IO,370)CSTLP
    DEL1=1.0D0/F1/PTS1*WTS1+DELAY1
    DEL2=1.0D0/F2/PTS2*WTS2+DELAY2
    W1=2.0D0*PI*F1
    W2=2.0D0*PI*F2
    BW=2.0D0*PI*(FC2-FC1)
    WO=2.0D0*PI*DSQRT(FC2*FC1)
    WOSQ=WO**2
```

```
      PHASE=W1*TAW1
      WRITE(IO,60)
      DO 70 J=1,MLP
      WRITE(IO,80)J,DLPRT(J)
   70 CLPRT(J)=DLPRT(J)/DCMPLX(CNORM,0.0D0)
      GAINLP=CSTLP/CNORM**MLP
      WRITE(IO,90)
      DO 100 J=1,MLP
      CLPRT(J)=CLPRT(J)*BW
  100 WRITE(IO,80)J,CLPRT(J)
      GAINBP=GAINLP*BW**MLP
      WRITE(IO,380)GAINBP
      WRITE(IO,110)
      DO 120 J=1,MLP
      JD=2*J
      JO=JD-1
      ARG(J)=CDSQRT(CLPRT(J)**2-4.0D0*WOSQ)
      CBPRT(JO)=(CLPRT(J)+ARG(J))/2.0D0
      CBPRT(JD)=(CLPRT(J)-ARG(J))/2.0D0
      CHECK(JO)=CBPRT(JO)**2-CLPRT(J)*CBPRT(JO)+WOSQ
      CHECK(JD)=CBPRT(JD)**2-CLPRT(J)*CBPRT(JD)+WOSQ
  120 WRITE(IO,130)J,ARG(J),CBPRT(JO),CBPRT(JD)
      WRITE(IO,330)
      DO 340 J=1,MBP
  340 WRITE(IO,80)J,CHECK(J)
      IF(NPASS.NE.0) GO TO 351
      READ(5,50)GAINBP
      WRITE(IO,352)GAINBP
  351 IF(IPASS.NE.0) GO TO 341
      WRITE(IO,342)
      DO 343 J=1,MBP
      READ(5,30)CBPRT(J)
      WRITE(IO,344)CBPRT(J)
  343 CONTINUE
  341 MSM=MBP+2
      OMEGA=W2
  180 CBPRT(MBP+1)=DCMPLX(0.0D0,OMEGA)
      CBPRT(MBP+2)=DCMPLX(0.0D0,-OMEGA)
      IF(OMEGA.EQ.W1) GO TO 400
      DO 401 J=1,MSM
  401 HFR(J)=CBPRT(J)
      GO TO 402
  400 DO 403 J=1,MSM
  403 LFR(J)=CBPRT(J)
  402 CONTINUE
      DO 140 I=1,MSM
      DEN=(1.0D0,0.0D0)
      LOP=CBPRT(I)
      NUMC=GAINBP*LOP**(MLP+1)
      NUMS=GAINBP*OMEGA*LOP**MLP
      WRITE(IO,310)LOP,DEN
```

```
      DO 150 J=1,MSM
      IF(J.EQ.I) GO TO 150
      CFACT=LOP-CBPRT(J)
      DEN=DEN*CFACT
      WRITE(IO,320)CFACT,DEN
  150 CONTINUE
      IF(OMEGA.EQ.W1) GO TO 160
      CCH(I)=NUMC/DEN
      CSH(I)=NUMS/DEN
      GO TO 140
  160 CCL(I)=NUMC/DEN
      CSL(I)=NUMS/DEN
  140 CONTINUE
      IF(OMEGA.EQ.W1) GO TO 170
      OMEGA=W1
      GO TO 180
  170 WRITE(IO,190)
      DO 200 J=1,MSM
  200 WRITE(IO,210)J,CCL(J),CSL(J),CCH(J),CSH(J)
      WRITE(IO,404)
      DO 405 J=1,MSM
  405 WRITE(IO,210)J,LFR(J),HFR(J)
      IL=0
      IH=0
      MSMM=MSM-1
      DO 406 J=1,MSMM
      JJ=J+1
      DO 407 I=JJ,MSM
      IF(RL(1,J).NE. RL(1,I).AND.
     /   RL(2,J).NE.-RL(2,I)) GO TO 407
      IL=IL+1
      AMPCL(IL)=2.0D0*CDABS(CCL(J))
      AMPSL(IL)=2.0D0*CDABS(CSL(J))
      ALPHL(IL)=RL(1,J)
      IF(RL(2,J).GT.0.0) GO TO 450
      RL(2,J)=-RL(2,J)
      CL(2,J)=-CL(2,J)
      SL(2,J)=-SL(2,J)
  450 BETAL(IL)=RL(2,J)
      PHICL(IL)=DATAN2(CL(2,J),CL(1,J))
      PHISL(IL)=DATAN2(SL(2,J),SL(1,J))
      GO TO 408
  407 CONTINUE
  408 DO 409 K=JJ,MSM
      IF(RH(1,J).NE. RH(1,K).AND.
     /   RH(2,J).NE.-RH(2,K)) GO TO 409
      IH=IH+1
      AMPCH(IH)=2.0D0*CDABS(CCH(J))
      AMPSH(IH)=2.0D0*CDABS(CSH(J))
      ALPHH(IH)=RH(1,J)
      IF(RH(2,J).GT.0.0) GO TO 460
      RH(2,J)=-RH(2,J)
```

```
      CH(2,J)=-CH(2,J)
      SH(2,J)=-SH(2,J)
  460 BETAH(IH)=RH(2,J)
      PHICH(IH)=DATAN2(CH(2,J),CH(1,J))
      PHISH(IH)=DATAN2(SH(2,J),SH(1,J))
      GO TO 406
  409 CONTINUE
  406 CONTINUE
      WRITE(IO,501)IL,IH
      WRITE(IO,507)W1,W2
      WRITE(IO,502)
      DO 503 J=1,IL
      WRITE(IO,504)AMPCL(J),AMPSL(J),ALPHL(J),
     /BETAL(J),PHICL(J),PHISL(J)
  503 CONTINUE
      WRITE(IO,505)
      DO 506 J=1,IH
      WRITE(IO,504)AMPCH(J),AMPSH(J),ALPHH(J),
     /BETAH(J),PHICH(J),PHISH(J)
  506 CONTINUE
      LA=TAW2.LT.TAW1
      SST=DSIN(W1*TAW1)
      CST=DCOS(W1*TAW1)
      WRITE(IO,651)
      WRITE(6,651)
  651 FORMAT(3X,'TIME',2X,'ENVRT',2X,'EPHRT',4X,'CR1',4X,'SR1',
     14X,'CR2',4X,'SR2',4X,'CR3',4X,'SR3',2X,'EPHDT')
  640 CR1=0.0
      SR1=0.0
      CR2=0.0
      SR2=0.0
      CR3=0.0
      SR3=0.0
      CRD=0.0
      SRD=0.0
      LC=TIME.LT.TAW1
      IF(TIME.GT.TAW2) GO TO 650
      PHR=BETAH(IL)*TIME
      PHADD=BETAH(IH)*TAW1
      DO 600 I=1,IL
      PHL=BETAL(I)*TIME
      ATL=DEXP(ALPHL(I)*TIME)
      EPC=PHL-PHR+PHICL(I)-PHICH(IL)+PHADD
      CTRMC=ATL*AMPCL(I)*DCOS(EPC)
      STRMC=ATL*AMPCL(I)*DSIN(EPC)
      CR1=CR1+CTRMC
      SR1=SR1+STRMC
      EXFRQ=BETAL(I)-BETAH(IH)
      CRD=CRD+ALPHL(I)*CTRMC-EXFRQ*STRMC
      SRD=SRD+ALPHL(I)*STRMC+EXFRQ*CTRMC
  600 CONTINUE
      IF(LC) GO TO 610
```

```
      TIM1=TIME-TAW1
      PHR=BETAH(IL)*TIM1
      DO 620 I=1,IL
      PHL=BETAL(I)*TIM1
      ATL=DEXP(ALPHL(I)*TIM1)
      EPC=PHL-PHR+PHICL(I)-PHICH(IL)
      EPS=PHL-PHR+PHISL(I)-PHICH(IL)
      CTRMC=ATL*CST*AMPCL(I)*DCOS(EPC)
      CTRMS=ATL*SST*AMPSL(I)*DCOS(EPS)
      STRMC=ATL*CST*AMPCL(I)*DSIN(EPC)
      STRMS=ATL*SST*AMPSL(I)*DSIN(EPS)
      CR2=CR2+CTRMS-CTRMC
      SR2=SR2+STRMS-STRMC
      EXFRQ=BETAL(I)-BETAH(IH)
      CRD=CRD+ALPHL(I)*(CTRMS-CTRMC)-EXFRQ*(STRMS-STRMC)
      SRD=SRD+ALPHL(I)*(STRMS-STRMC)+EXFRQ*(CTRMS-CTRMC)
  620 CONTINUE
      DO 630 I=1,IH
      PHH=BETAH(I)*TIM1
      ATH=DEXP(ALPHH(I)*TIM1)
      EPC=PHH-PHR+PHICH(I)-PHICH(IH)
      EPS=PHH-PHR+PHISH(I)-PHICH(IH)
      CTRMC=ATH*CST*AMPCH(I)*DCOS(EPC)
      CTRMS=ATH*SST*AMPSH(I)*DCOS(EPS)
      STRMC=ATH*CST*AMPCH(I)*DSIN(EPC)
      STRMS=ATH*SST*AMPSH(I)*DSIN(EPS)
      CR3=CR3+CTRMC-CTRMS
      SR3=SR3+STRMC-STRMS
      EXFRQ=BETAH(I)-BETAH(IH)
      CRD=CRD+ALPHH(I)*(CTRMC-CTRMS)-EXFRQ*(STRMC-STRMS)
      SRD=SRD+ALPHH(I)*(STRMC-STRMS)+EXFRQ*(CTRMC-CTRMS)
  630 CONTINUE
  610 CONTINUE
      CRT=CR1+CR2+CR3
      SRT=SR1+SR2+SR3
      ENVRT=DSQRT(CRT*CRT+SRT*SRT)
      EPHRT=DATAN2(SRT,CRT)
      EPHDT=(CRT*SRD-SRT*CRD)/(SRT*SRT+CRT*CRT)
      WRITE(10,621)TIME,ENVRT,EPHRT,CR1,SR1,CR2,SR2,CR3,SR3,EPHDT
      WRITE(6,621)TIME,ENVRT,EPHRT,CR1,SR1,CR2,SR2,CR3,SR3,EPHDT
      TIME=TIME+DELT
      GO TO 640
  621 FORMAT(' ',10F7.4)
  650 WRITE(6,710)
  710 FORMAT(' DO YOU WISH TO CONTINUE?')
      READ(5,711)IANS
  711 FORMAT(A4)
      IF(IANS-IYES)660,670,660
  660 STOP
      END
```

APPENDIX 3

THE AVERAGE SPECTRAL DISTRIBUTION OF THE FSK SIGNAL

If it is assumed that over a transmission link all possible messages will be sent, and that at any chosen time it is equally likely that any one of all the possible messages will be sent, then a frequency distribution can be defined which is based on the average over all these possible messages. Although a message may deviate considerably from the average, it would appear reasonable that the average should be used as one basis for formulating the bandwidth requirement of any particular transmission system [27,28].

In the present r.f. link, information is transmitted by switching between two frequencies ω_1 and ω_2 (say) representing the binary digits '0' and '1' respectively. The rate of occurrence of each frequency is known to be the same since the data have a balanced-code format for transmission (cf. sect. 3.2 above). Specifically, the binary-code digits '1' and '0' are transmitted as the balanced-code combinations '10' and '01' respectively.

The spectrum of the transmitted FSK signal $X_s(\omega)$ (say) may be obtained by a summation of the spectra associated with the transmission of the individual binary-coded digits of period 2T (say). Thus

$$X_s(\omega) = \sum_{r=o}^{N} \left\{ a_r F_{1r}(\omega) \exp(-j\omega 2rT) + (1-a_r) F_{or}(\omega) \exp(-j\omega 2rT) \right\} \quad \ldots\ldots(A3.1)$$

where/

where a_r takes the value 0 or 1 representing the value of the r-th binary-coded digit, and

$$F_{1r}(\omega) \equiv \int_o^T \sin(\omega_2 t + \phi_r)\exp(-j\omega t)dt + \int_T^{2T} \sin(\omega_1 t + \phi_r + \overline{\omega_2 - \omega_1}\, T)\exp(-j\omega t)dt \quad \ldots(A3.2),$$

$$F_{or}(\omega) \equiv \int_o^T \sin(\omega_1 t + \phi_r)\exp(-j\omega t)dt + \int_T^{2T} \sin(\omega_2 t + \phi_r + \overline{\omega_1 - \omega_2}\, T)\exp(-j\omega t)dt \quad \ldots(A3.3),$$

in which $$\phi_r = \phi_o + r(\omega_1 + \omega_2)T \quad \ldots\ldots(A3.4).$$

For the purpose of analysis, it is assumed that the binary-coded data are random, which in turn implies that $\overline{a}_r = \frac{1}{2}$.

The average power spectral distribution $W_s(\omega)$ of the transmitted signal is defined [27,28] in terms of $X_s(\omega)$ by the expression

$$W_s(\omega) = \frac{1}{T} \lim_{N\to\infty} \frac{1}{N+1} \overline{\left|X_s(\omega)\right|^2} \quad \ldots\ldots(A3.5).$$

The determining function $\overline{\left|X_s(\omega)\right|^2}$ has been analysed in the literature [27,28] for a random binary-coded data stream and may be written/

written

$$\overline{\left|X_s(\omega)\right|^2} = \sum_{r=o}^{N} \tfrac{1}{4}\left|F_{1r}(\omega) - F_{or}(\omega)\right|^2$$

$$+ \sum_{r=o}^{N}\sum_{x=o}^{N} \tfrac{1}{4}\left\{F_{1r}(\omega) + F_{or}(\omega)\right\}\left\{F_{1x}^{*}(\omega) + F_{ox}^{*}(\omega)\right\}\exp\left\{-j\omega 2(r-x)T\right\} \qquad .....(A3.6)$$

where x is a dummy variable and * denotes the complex conjugate function. Further simplification of expression (A3.6) depends on isolating and summing the terms containing the phase component ϕ_r.

From expressions (A3.2) and (A3.3), it can be shown that

$$F_{1r}(\omega) = \cos\phi_r\, F_{1s}(\omega) + \sin\phi_r\, F_{1c}(\omega) \qquad .....(A3.7),$$

$$F_{or}(\omega) = \cos\phi_r\, F_{os}(\omega) + \sin\phi_r\, F_{oc}(\omega) \qquad .....(A3.8),$$

where

$$\begin{matrix} F_{1s} \\ F_{1c} \end{matrix}(\omega) \equiv \int_o^T \begin{matrix}\sin \\ \cos\end{matrix}(\omega_2 t)\exp(-j\omega t)dt + \int_T^{2T} \begin{matrix}\sin \\ \cos\end{matrix}(\omega_1 t + \omega_2 T - \omega_1 T)\exp(-j\omega t)dt \qquad .....(A3.9),$$

$$\begin{matrix} F_{os} \\ F_{oc} \end{matrix}(\omega) \equiv \int_o^T \begin{matrix}\sin \\ \cos\end{matrix}(\omega_1 t)\exp(-j\omega t)dt + \int_T^{2T} \begin{matrix}\sin \\ \cos\end{matrix}(\omega_2 t + \omega_1 T - \omega_2 T)\exp(-j\omega t)dt \qquad .....(A3.10).$$

The form of $F_{1r}(\omega)$ and $F_{or}(\omega)$ [given by eqns. (A3.7) and (A3.8) respectively] implies that the evaluation of $\overline{\left|X_s(\omega)\right|^2}$ requires the summing of terms composed of the products and cross-products of $\sin\phi_r$ and $\cos\phi_r$.

$$\bar{\Sigma}_r \cos\phi_r \cos\phi_x = 0 \quad (x \neq r)$$

$$= \tfrac{1}{2} \quad (x = r)$$

$$\bar{\Sigma}_r \sin\phi_r \sin\phi_x = 0 \quad (x \neq r)$$

$$= \tfrac{1}{2} \quad (x = r)$$

and $$\bar{\Sigma}_r \cos\phi_r \sin\phi_x = 0 \qquad \text{.....(A3.11).}$$

$\bar{\Sigma}$ signifying $\lim_{N \to \infty} \frac{1}{N+1} \sum_{r=0}^{N}$. It follows[27] that in general

$$W_s(\omega) \simeq \frac{1}{8\pi} \left\{ \left| F_{1s}(\omega) - F_{os}(\omega) \right|^2 + \left| F_{1c}(\omega) - F_{oc}(\omega) \right|^2 \right\}$$

.....(A3.12)

$$\simeq \frac{1}{8\pi} \left\{ \left| F_{1s}(\omega) \right|^2 + \left| F_{os}(\omega) \right|^2 + \left| F_{1c}(\omega) \right|^2 + \left| F_{oc}(\omega) \right|^2 \right\}$$

.....(A3.13).

Evaluating[79,80] the integrals defined by expressions (A3.9) and (A3.10), we find that

$$\left| F_{1s}(\omega) \right|^2 + \left| F_{os}(\omega) \right|^2 + \left| F_{1c}(\omega) \right|^2 + \left| F_{oc}(\omega) \right|^2 \qquad \text{.....(A3.14)}$$

$$= \frac{T^2}{4} \left[Sa^2\{(\omega + \omega_2)T/2\} + Sa^2\{(\omega - \omega_2)T/2\} \right.$$

$$\left. + Sa^2\{(\omega + \omega_1)T/2\} + Sa^2\{(\omega - \omega_1)T/2\} \right] \qquad \text{.....(A3.15),}$$

where $$Sa(x) \equiv \sin(x)/x \qquad \text{.....(A3.16).}$$

Accordingly, certain discrete frequencies excepted,[27]

$$W_s(\tilde{\omega}) \simeq \frac{T}{32} \left[Sa^2\{(\omega + \omega_2)T/2\} + Sa^2\{(\omega - \omega_2)T/2\} \right.$$

$$\left. + Sa^2\{(\omega + \omega_1)T/2\} + Sa^2\{(\omega - \omega_1)T/2\} \right] \qquad \text{.....(A3.17).}$$

APPENDIX 4

ANALYSIS OF AUTOMATIC FREQUENCY CONTROL*

The FSK detector/FM receiver is schematically represented in fig. A4.1 and may be regarded as a conventional (open-loop) receiver or an AFC receiver depending on whether the switch S is open or closed. Two channels may be defined, viz.

(i) the i.f. channel which starts at the mixer output and ends at the discriminator input, and

(ii) the feedback channel which starts at the discriminator output and ends at the voltage-controlled oscillator input.

A useful analogue[34,35] of such a receiver is the 'phase-function analogue'. This analogue deals with the excess-phase (i.e. phase in excess of the carrier phase) of the system waveforms. In such an analogue, the mixer may be regarded as a conventional summing device with a negative-input terminal. This is shown in fig. A4.2. [In this figure $\Phi_r(s)$, $\Phi_i(s)$ and $\Phi_o(s)$ represent the Laplace transforms of the excess-phase functions $\phi_r(t)$, $\phi_i(t)$ and $\phi_o(t)$ respectively and $V_d(s)$ represents the Laplace transform of the discriminator output voltage $v_d(t)$.]

The summing property of the mixer may be derived quite simply by writing the total instantaneous phases $\theta_r(t)$, $\theta_o(t)$ and $\theta_i(t)$ of the r.f., local oscillator, and i.f. waves respectively in the form/

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*The analysis presented in this appendix is adapted from an analysis of FM feedback given by Subaran[34].

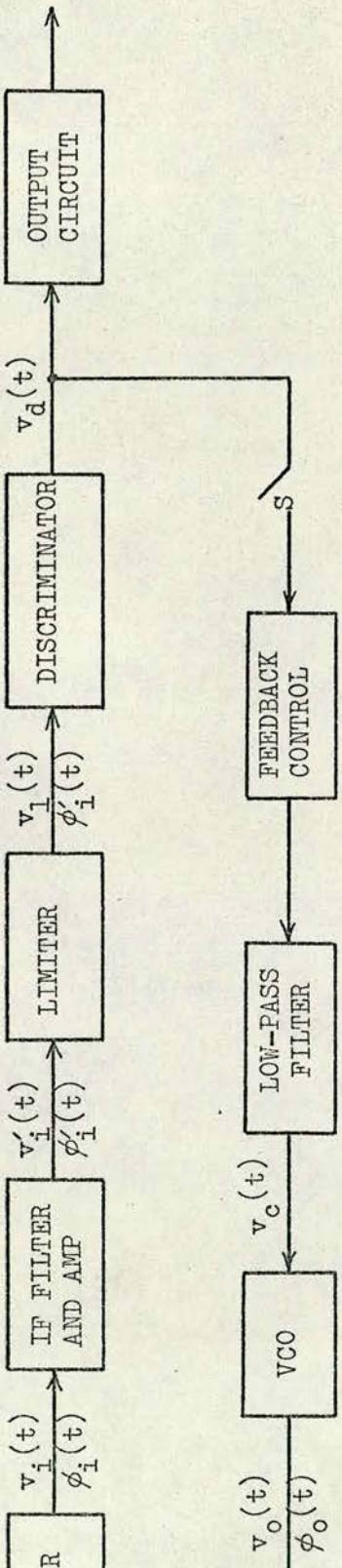

Fig. A4.1 Block diagram of the FM receiver/FSK detector.

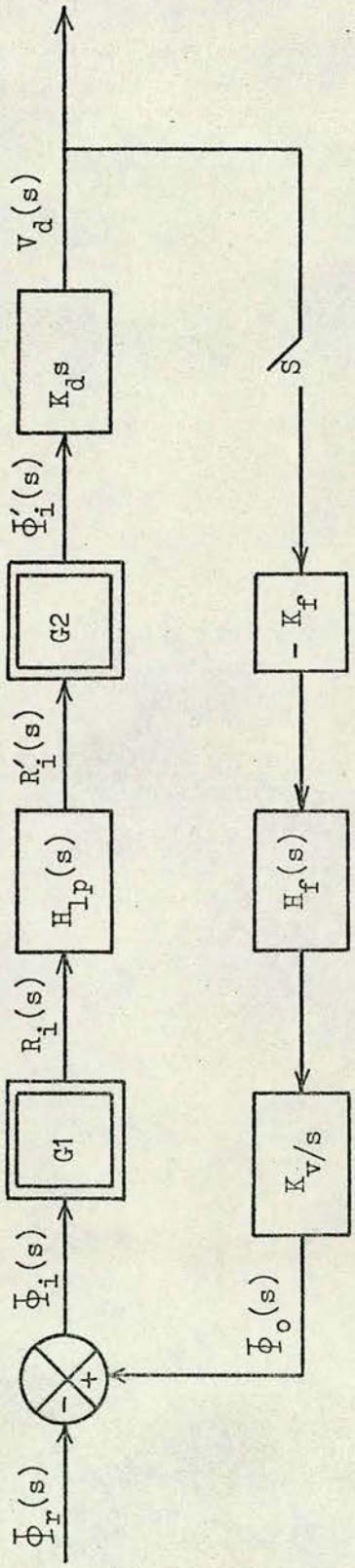

Fig. A4.2 'Phase-function' analogue of the FM receiver/FSK detector.

$$\theta_r(t) = \omega_r t + \phi_r(t) \quad ; \quad \theta_o = \omega_o t + \phi_o(t)$$

$$\text{and} \quad \theta_i(t) = \omega_i t + \phi_i(t) \qquad \text{.....(A4.1).}$$

The total instantaneous phase of each wave may be regarded as comprising a linearly-varying 'carrier' term and an 'information' excess-phase term. In the present receiver system with high-side-beat mixing, the instantaneous frequency $\dot{\theta}_i(t)$ of the i.f. wave is the difference between the instantaneous frequencies $\dot{\theta}_o(t)$ and $\dot{\theta}_r(t)$ of the local oscillator and r.f. waves. Thus

$$\omega_i + \dot{\phi}_i(t) = \omega_o - \omega_r + \dot{\phi}_o(t) - \dot{\phi}_r(t) \qquad \text{.....(A4.2),}$$

and so, on setting $\omega_i = \omega_o - \omega_r$,

$$\dot{\phi}_i(t) = \dot{\phi}_o(t) - \dot{\phi}_r(t) \quad ; \quad \phi_i(t) = \phi_o(t) - \phi_r(t) \text{.....(A4.3).}$$

Accordingly, the mixer is seen to produce an i.f. excess phase $\phi_i(t)$ which is the difference between the excess phases $\phi_o(t)$ and $\phi_r(t)$ of the local oscillator and r.f. waves respectively.

Voltage amplification and voltage limiting in the i.f. channel will not directly manifest themselves in the excess-phase analogue of the receiver. This may be demonstrated by writing the i.f. wave $v_i(t)$ at the output of the mixer in the complex form

$$v_i(t) = A_i \exp[j \{\omega_i t + \phi_i(t)\}] \qquad \text{.....(A4.4),}$$

where A_i is the amplitude of the i.f. wave at the output of the mixer. After broad-band amplification, filtering and limiting in the i.f. channel, the wave $v_1(t)$ at the input to the discriminator is/

is given by

$$v_1(t) = A_1 \exp[j\{\omega_i t + \phi_i'(t)\}] \qquad \ldots\ldots(A4.5),$$

where A_1 is the output level produced by the limiter and is constant in practice, and $\phi_i'(t)$ is determined by the i.f. filtering.

In the present design, the phase-locked-loop discriminator transfer gain K_d is independent of the input signal amplitude A_1, provided that $A_1 > 100mV$ [which is always the case for practical reception (cf. subsection 4.2.2 above)]. Accordingly, the PLLD essentially acts as a balanced phase differentiator which produces at its output the derivative of the input excess-phase function. [The PLLD transfer function is broad-band and produces no significant filtering effect in comparison with the i.f. filter (cf. sect. 4.2 above).]

In the discriminator, the excess-phase function is converted to an output voltage function $v_d(t)$ which, in an open loop system, is delivered to some output circuit. In the feedback receiver, this circuit is placed outside the loop and need not be regarded as part of the analogue.

The feedback channel provides conventional amplification and filtering of the discriminator output voltage. The broad-band feedback-gain control unit regulates the amount of feedback applied, and the low-pass filter $H_f(s)$ represents all the feedback control filtering. [We note here that a gain inversion is required for operation with high-side-beat mixing.]

The voltage-controlled oscillator essentially acts as an FM generator. If the input to the oscillator is $v_c(t)$, the excess-phase function $\phi_o(t)$ at the output and $v_c(t)$ are related through

$$\phi_o(t) = K_v \int_o^t v_c(t)dt \qquad .....(A4.6),$$

where K_v is the transfer gain of the voltage-controlled-oscillator. In the phase-function analogue of the receiver, the voltage-controlled oscillator performs the function of an integrator and may therefore be represented as a device having a transfer function K_v/s.

To determine the effect of the i.f. filter on the phase-function analogue, we express the filter input $v_i(t)$ and output $v_i'(t)$ in the form

$$v_i(t) = r_i(t) \exp(j\omega_i t) \;\; ; \;\; r_i(t) \equiv \exp\left\{j\phi_i(t)\right\} \qquad .....(A4.7);$$

$$v_i'(t) = r_i'(t) \exp(j\omega_i t) \;\; ; \;\; r_i'(t) \equiv \exp\left\{j\phi_i'(t)\right\} \qquad .....(A4.8);$$

where we have omitted the amplitudes of the $v_i(t)$ and $v_i'(t)$ waves. If $V_i(s)$, $V_i'(s)$, $R_i(s)$ and $R_i'(s)$ are the Laplace transforms of $v_i(t)$, $v_i'(t)$, $r_i(t)$ and $r_i'(t)$ respectively, then it can be shown that [50, 51, 52, 53],

$$V_i(s) = R_i(s - j\omega_i) \;\; ; \;\; V_i'(s) = R_i'(s - j\omega_i) \qquad .....(A4.9);$$

where $R_i(s - j\omega_i)$ and $R_i'(s - j\omega_i)$ are the Laplace transforms of $R_i(s)$ and $R_i'(s)$ shifted upwards along the frequency axis by amount ω_i. $V_i(s)$ and $V_i'(s)$ are related through the transfer function $H_{bp}(s)$ of the i.f. filter. Thus

$$R_i'(s - j\omega_i) = R_i(s - j\omega_i)\, H_{bp}(s) \qquad .....(A4.10),$$

and/

and replacing the variable $(s - j\omega_i)$ by the variable s gives

$$R_i'(s) = R_i(s)\, H_{bp}(s + j\omega_i) = R_i(s)\, H_{lp}(s) \qquad .....(A4.11).$$

$H_{bp}(s + j\omega_i)$ $[= H_{lp}(s)]$ is the transfer function $H_{bp}(s)$ of the i.f. filter shifted downwards along the frequency axis by amount ω_i (i.e. it is the transfer function of the low-pass analogue of the i.f. filter).

In general, the relationship in eqn. (A4.7) between the the phase function $\phi_i(t)$ and $r_i(t)$ is nonlinear, and it is not possible to relate the Laplace transform $\Phi_i(s)$ of $\phi_i(t)$ to the Laplace transform $R_i(s)$ of $r_i(t)$ through a linear transfer function. Similar remarks must, of course, apply to $r_i'(t)$, $\phi_i'(t)$, $R_i'(s)$ and $\Phi'(s)$. Accordingly, the effect of the i.f. filter or the phase-function analogue can only be taken into account by the inclusion of two 'function generators' G1 and G2. This is shown in fig. A4.2 where G1 having input $\Phi_i(s)$ produces output $R_i(s)$. G2 may be regarded as performing the inverse operation of producing an output $\Phi_i'(s)$ for an input $R_i'(s)$.

The two nonlinear elements G1 and G2 make the phase-function analogue unsuitable for analysis with the usual techniques. However, it may be simplified for specific applications.

In particular, the requirements for AFC are that the feedback channel should block all modulation effects and pass only a signal indicating a slow change in the i.f. frequency. Accordingly, the i.f. channel (the bandwidth of which is chosen to pass all modulation effects)/

effects) can be considered to be broad-band in comparison with the feedback channel. For AFC analysis, therefore, we assume that $v_i(t) = v_i'(t)$ (i.e. the i.f. filter input and output signals are the same). In turn, this implies that $\Phi_i(s) = \Phi_i'(s)$.

The simplified phase-function analogue for AFC analysis is given in fig. A4.3. The individual gains K_d, K_f and K_v (of the discriminator, feedback control, and voltage-controlled oscillator respectively) may be lumped as a single loop gain $G_a (= K_d K_f K_v)$. The following closed-loop transfer functions may be written

$$\Phi_i(s)/\Phi_r(s) = -1/\{1 + G_a H_f(s)\} \qquad .....(A4.12),$$

and

$$\Phi_o(s)/\Phi_r(s) = G_a H_f(s)/\{1 + G_a H_f(s)\} \qquad .....(A4.13).$$

Stable closed-loop operation is ensured[49] by making $H_f(s)$ a single-pole low-pass filter of the form

$$H_f(s) = 1/(1 + s\tau) \qquad .....(A4.14)$$

[i.e. the open-loop gain $G_a H_f(s)$ crosses the OdB axis at -6dB per octave]. Substituting for $H_f(s)$ in equation (A4.12) gives

$$\frac{\Phi_i(s)}{\Phi_r(s)} = \frac{-1}{(1 + G_a)} \frac{(1 + s\tau)}{\{1 + s\tau/(1 + G_a)\}} \qquad .....(A4.15),$$

from which it is evident that in the steady state a variation $\Delta\phi_r$ in $\phi_r(t)$ produces a variation in $\phi_i(t)$ of magnitude $\Delta\phi_i = -\Delta\phi_r/(1 + G_a)$. Accordingly, a drift in r.f. frequency of magnitude $\Delta\dot{\phi}_r$ is reduced by a factor $1 + G_a$ and appears as a drift in i.f. frequency of magnitude $\Delta\dot{\phi}_i = -\Delta\dot{\phi}_r/(1 + G_a)$.

Variations in the local-oscillator frequency are also reduced by the closed-loop operation. In fig. A4.3, a change in the excess-phase function of the local-oscillator waveform is represented by the additional input $\mathcal{L}\phi_o'(s)$ to the summer. The closed-loop transfer functions corresponding to equations (A4.12) and (A4.13) may be written

$$\mathcal{L}\phi_i(s)/\mathcal{L}\phi_o'(s) = 1/\{1 + G_a H_f(s)\} \qquad .....(A4.16)$$

and

$$\mathcal{L}\phi_o(s)/\mathcal{L}\phi_o'(s) = -G_a H_f(s)/\{1 + G_a H_f(s)\} \qquad .....(A4.17).$$

Substituting for $H_f(s)$ in eqn. (A4.16) according to eqn. (A4.14) gives

$$\frac{\mathcal{L}\phi_i(s)}{\mathcal{L}\phi_o'(s)} = \frac{1}{(G_a + 1)} \frac{(1 + s\tau)}{\{1 + s\tau/(1 + G)\}} \qquad .....(A4.18),$$

from which it is evident that in the steady-state a variation $\Delta\phi_o'$ in $\phi_o'(t)$ produces a variation in $\phi_i(t)$ of magnitude $\Delta\phi_i = \Delta\phi_o'/(1 + G_a)$. Accordingly, a drift in local-oscillator frequency of magnitude $\Delta\dot{\phi}_o'$ is reduced by a factor $1 + G_a$ and appears as a drift in the i.f. frequency of magnitude $\Delta\dot{\phi}_i = \Delta\dot{\phi}_o'/(1 + G_a)$.

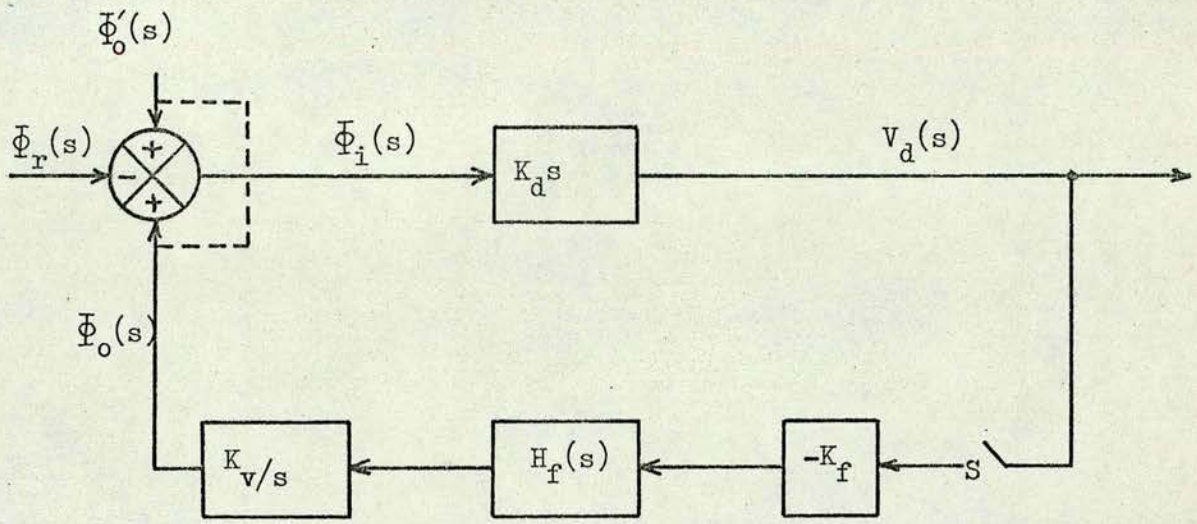

Fig. A4.3 'Phase-function' analogue for AFC analysis.

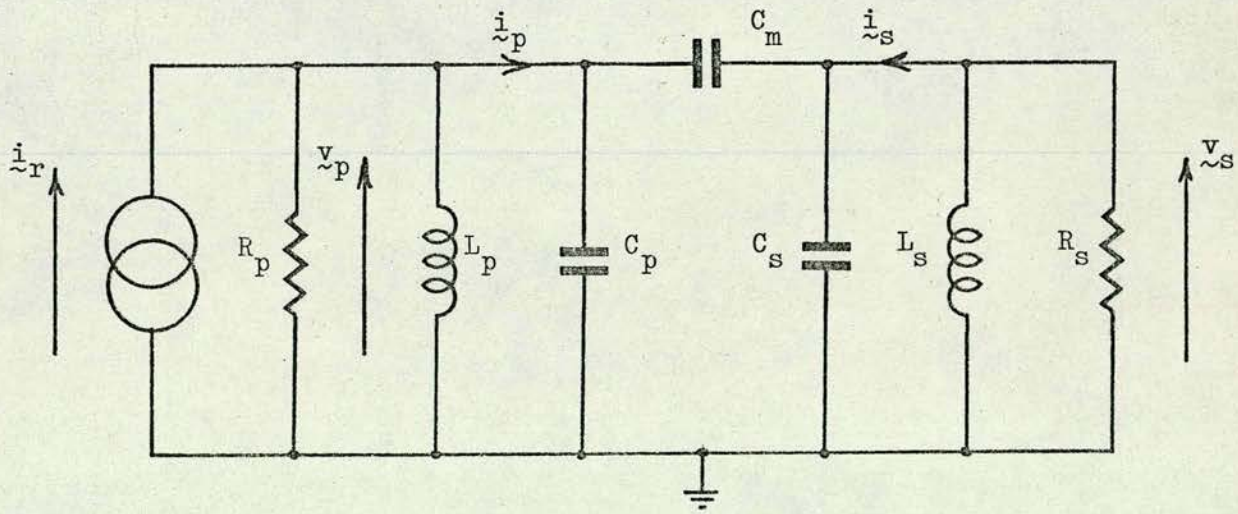

Fig. A5.1 The capacitor top-coupled tuned circuit.

APPENDIX 5

ANALYSIS OF CAPACITOR TOP-COUPLED CIRCUITS

The capacitor top-coupled circuit is illustrated in fig. A5.1.

[The symbolic notation $\underset{\sim}{x}$ denotes that the variable x is a phasor.]

We consider the analysis of this circuit as follows:

The circuit equations may be written

$$\underset{\sim}{i}_r = \underset{\sim}{v}_p \left(\frac{1}{R_p} + \frac{1}{j\omega L_p}\right) + \underset{\sim}{i}_p \qquad \text{.....(A5.1)},$$

$$0 = \underset{\sim}{v}_s \left(\frac{1}{R_s} + \frac{1}{j\omega L_s}\right) + \underset{\sim}{i}_s \qquad \text{.....(A5.2)},$$

$$\underset{\sim}{i}_p = \underset{\sim}{v}_p\, j\omega C_p + (\underset{\sim}{v}_p - \underset{\sim}{v}_s) j\omega C_m \qquad \text{.....(A5.3)},$$

$$\underset{\sim}{i}_s = \underset{\sim}{v}_s\, j\omega C_s + (\underset{\sim}{v}_s - \underset{\sim}{v}_p) j\omega C_m \qquad \text{.....(A5.4)},$$

Equations (A5.3) and (A5.4) imply that the coupling coefficient [81,82] k of this circuit is given by

$$k^2 = C_m^2/(C_m + C_p)(C_m + C_s) \qquad \text{.....(A5.5)}.$$

Substituting for $\underset{\sim}{i}_p$ and $\underset{\sim}{i}_s$ in equations (A5.1) and (A5.2) according to equations (A5.3) and (A5.4) gives

$$\underset{\sim}{i}_r = \underset{\sim}{v}_p\left[\frac{1}{R_p} + j\left\{\omega(C_p + C_m) - \frac{1}{\omega L_p}\right\}\right] - \underset{\sim}{v}_s j\omega C_m \qquad \text{.....(A5.6)},$$

$$\text{and } 0 = \underset{\sim}{v}_s\left[\frac{1}{R_s} + j\left\{\omega(C_s + C_m) - \frac{1}{\omega L_s}\right\}\right] - \underset{\sim}{v}_p j\omega C_m \qquad \text{.....(A5.7)}.$$

In order to simplify equations (A5.6) and (A5.7) we postulate that the primary and secondary tuned circuits have the common resonance frequency ω_c, where/

where

$$\omega_c^2 = \frac{1}{L_p(C_m + C_p)} = \frac{1}{L_s(C_m + C_s)} \qquad \text{.....(A5.8).}$$

The Q-factors Q_p and Q_s, associated respectively with the primary and secondary parallel-tuned circuits at resonance, may then be written

$$Q_p = \frac{R_p}{\omega_c L_p} \quad ; \quad Q_s = \frac{R_s}{\omega_c L_s} \qquad \text{.....(A5.9).}$$

Accordingly, equations (A5.6) and (A5.7) may be rewritten respectively in the form

$$\underset{\sim}{i}_r = \frac{\underset{\sim}{v}_p}{R_p}(1 + jQ_p\delta_\omega) - \underset{\sim}{v}_s j\omega C_m \qquad \text{.....(A5.10),}$$

$$\text{and} \qquad 0 = \frac{\underset{\sim}{v}_s}{R_s}(1 + jQ_s\delta_\omega) - \underset{\sim}{v}_p j\omega C_m \qquad \text{.....(A5.11),}$$

$$\text{in which} \qquad \delta_\omega \equiv \frac{\omega}{\omega_c} - \frac{\omega_c}{\omega} \qquad \text{.....(A5.12).}$$

Equations (A5.10) and (A5.11) may be solved for the circuit transfer gain $\underset{\sim}{v}_s/\underset{\sim}{i}_r$ and input impedance $\underset{\sim}{v}_p/\underset{\sim}{i}_r$. Thus

$$\underset{\sim}{v}_s/\underset{\sim}{i}_r = j\Big/\omega C_m \cdot \left\{1 + \frac{(1 + jQ_s\delta_\omega)(1 + jQ_p\delta_\omega)}{\omega^2 C_m^2 R_p R_s}\right\} \qquad \text{.....(A5.13),}$$

$$\underset{\sim}{v}_p/\underset{\sim}{i}_r = 1\Big/\frac{\omega^2 C_m^2 R_s}{(1 + jQ_s\delta_\omega)} \cdot \left\{1 + \frac{(1 + jQ_s\delta_\omega)(1 + jQ_p\delta_\omega)}{\omega^2 C_m^2 R_p R_s}\right\} \qquad \text{.....(A5.14).}$$

At the common tuned frequency ω_c, $\delta_\omega = 0$ and equation (A5.13) reduces to

$$\underset{\sim}{v}_s/\underset{\sim}{i}_r \Big|_{\omega=\omega_c} = j\Big/\omega_c C_m \cdot \left\{1 + \frac{1}{\omega_c^2 C_m^2 R_p R_s}\right\} \qquad \text{.....(A5.15).}$$

If all the quantities with the exception of C_m are kept constant, it can easily be shown that the maximum value of the transfer gain is achieved when

$$\omega_c^2 C_m^2 R_s R_p = 1 \qquad \text{.....(A5.16).}$$

This is the condition for optimum coupling. By substituting from equation (A5.5), therefore, the optimum coupling coefficient k_o is given by

$$k_o^2 = k^2 = 1/R_s R_p \omega_c^2 (C_m + C_s)(C_m + C_p) \qquad \text{.....(A5.17).}$$

Further manipulation of equations (A5.17), (A5.8) and (A5.9) reveals that k_o may also be expressed in terms of the Q-factors Q_s and Q_p as

$$k_o^2 = 1/Q_s Q_p \qquad \text{.....(A5.18).}$$

For critical coupling, equations (A5.13) and (A5.14) may be rewritten respectively as

$$\underset{\sim}{v}_s/\underset{\sim}{i}_r = \frac{j\omega}{\omega_c^2 C_m \left\{\frac{\omega^2}{\omega_c^2} + (1 + jQ_s\delta_\omega)(1 + jQ_b\delta_\omega)\right\}} \qquad \text{.....(A5.19),}$$

and

$$\underset{\sim}{v}_p/\underset{\sim}{i}_r = \frac{R_p(1 + jQ_s\delta_\omega)}{\left\{\frac{\omega^2}{\omega_c^2} + (1 + jQ_s\delta_\omega)(1 + jQ_p\delta_\omega)\right\}} \qquad \text{.....(A5.20).}$$

Equation (A5.20) defines the circuit input impedance Z_i $[= \underset{\sim}{v}_p/\underset{\sim}{i}_r]$. The circuit output impedance Z_o can be derived in a similar manner with the reference current source $\underset{\sim}{i}_r$ feeding the secondary tank.

Thus/

Thus

$$Z_o = \frac{R_s(1 + jQ_p\delta_\omega)}{\left\{\frac{\omega^2}{\omega_c^2} + (1 + jQ_s\delta_\omega)(1 + jQ_p\delta_\omega)\right\}} \qquad .....(A5.21).$$

Equation (A5.19), on the other hand, defines the band-pass characteristic of the capacitor top-coupled circuit with critical coupling. The 3dB (or half-power) bandwidth B_3 for critical coupling can be obtained simply [from equation (A5.19)] as [81,82]

$$B_3 \approx \sqrt{2}\, k_o f_c = \sqrt{2}\, f_c/\sqrt{(Q_s Q_p)} \quad (B_3 \ll f_c) \qquad .....(A5.22).$$

whenever $Q_s = Q_p$.

The approximation of (A5.22) holds for the present design in which the selectivity $f_c/B > 10$ (cf. subsection 4.2.1 above).

APPENDIX 6

THE AVERAGE SPECTRAL DISTRIBUTION OF THE BALANCED-CODE DATA

The average spectral distribution of the balanced-code data is derived in the same way as the average spectral distribution of the transmitted FSK data. [Appendix 3 refers.]

The balanced-code data have been shown (in sect. 3.2 above) to be comprised of a series of '10' and '01' code combinations representing the equivalent binary-code data bits '1' and '0' respectively. If the '1' and '0' bits of the balanced-code data are transmitted as +1 volt and -1 volt respectively and, furthermore, if the bit period of the equivalent binary-code data is 2T, then the transmitted balanced-code combination $d_c(t)$ corresponding to the equivalent r-th binary-code bit can be written

$$d_c(t) = (2a_r - 1)\left\{u(t) - 2u(t - T)\right\} \quad (0 < t \leqslant 2T) \quad \ldots\ldots(A6.1),$$

where a_r takes the value 0 or 1 corresponding to the value of the binary-code bits '0' and '1' respectively.

The spectrum $X_d(\omega)$ of the transmitted balanced-code data is found by summing the individual spectra associated with each code combination $d_c(t)$ given by equation (A6.1). Thus

$$X_d(\omega) = \sum_{r=o}^{N} \left\{a_r F_1(\omega) + (1 - a_r)F_o(\omega)\right\} \exp(-j\omega 2rT) \quad \ldots\ldots(A6.2)$$

where/

where

$$F_1(\omega) \equiv \int_0^T \exp(-j\omega t)dt - \int_T^{2T} \exp(-j\omega t)dt \qquad .....(A6.3)$$

$$= \frac{1}{j\omega}\left\{1 - \exp(-j\omega T)\right\}^2 \qquad .....(A6.4)$$

$$= \omega T^2 j\, Sa^2(\omega T/2)\exp(-j\omega T) \qquad .....(A6.5),$$

in which $Sa(x) = (\sin x)/x$ .....(A6.6);

and $F_o(\omega) = -F_1(\omega)$ .....(A6.7).

The average spectral distribution $W_d(\omega)$ of the balanced-code data is defined [27, 28] in terms of $X_d(\omega)$ by

$$W_d(\omega) = \frac{1}{T}\lim_{N\to\infty}\frac{1}{N+1}\overline{\left|X_d(\omega)\right|^2} \qquad .....(A6.8).$$

It is required, therefore, to evaluate $\left|X_d(\omega)\right|^2$ and then average. The general technique for evaluating $\overline{\left|X_d(\omega)\right|^2}$ has been described previously [27,28] and, assuming that the data are random (which implies that $\bar{a}_r = \frac{1}{2}$), may be written here

$$\overline{\left|X_d(\omega)\right|^2} = \sum_{r=o}^{N}\frac{1}{4}\left|F_1(\omega) - F_o(\omega)\right|^2 + \sum_{r=o}^{N}\sum_{s=o}^{N}\frac{1}{4}\left|F_1(\omega) + F_o(\omega)\right|^2 \exp\left\{-j\omega(r-s)T\right\} \qquad .....(A6.9),$$

where s is a dummy variable. This expression may be simplified by substituting for $F_1(\omega)$ and $F_o(\omega)$ according to equations (A6.5) and (A6.7). In turn, by substuting for $\overline{\left|X_d(\omega)\right|^2}$ in equation (A6.8), the average spectral density of the balanced-code data becomes

$$W_d(\omega) = \lim_{N\to\infty}\frac{1}{N+1}\sum_{r=o}^{N}\left\{\omega^2T^3\, Sa^4(\omega T/2)\right\} \qquad .....(A6.10).$$

APPENDIX 7

THE NOISE GENERATOR DESIGN*

An RCA 931A photo-multiplier tube[83] (referred to here as PM) is used as the noise source since such tubes are known [84,85] to be capable of producing high-level wide-band noise. [A high level of noise is required for test purposes so that any system noise signals will be small in comparison.]

The spectrum of PM noise has been shown [84] to be flat to within $\pm \frac{1}{2}$ dB up to 200 MHz. In this range, the mean-square shot-noise current i_n^2 at the anode of the PM is given approximately by

$$i_n^2 \approx 2\, e\, i_a\, B(g^{m+1} - 1)/(g - 1) \qquad \text{.....(A7.1)},$$

where e is the electronic charge ($= 1.6 \times 10^{-19}$ coulomb), i_a is the d.c. anode current, g is the gain per multiplier stage, m is the number of multiplier stages, and B is the system bandwidth in Hertz. Accordingly, for narrow system bandwidths within the 200 MHz range, the PM may be considered to produce noise with a Gaussian distribution.

A circuit diagram of the PM noise generator is given in fig. A7.1. For maximum noise current, it is required that the PM be run at maximum d.c. anode current and maximum gain [equation (A7.1) refers], the latter being dependent upon the anode-to-cathode voltage[83]. In the present design, the d.c. anode current is chosen to be 100 μA (=1/10 of the maximum rated value), this value being considered to give a good compromise between a high output noise level and longevity of the tube.

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*The design analysis of this appendix is obtained, in part, from the design of a Gaussian noise generator given by Subaran[34].

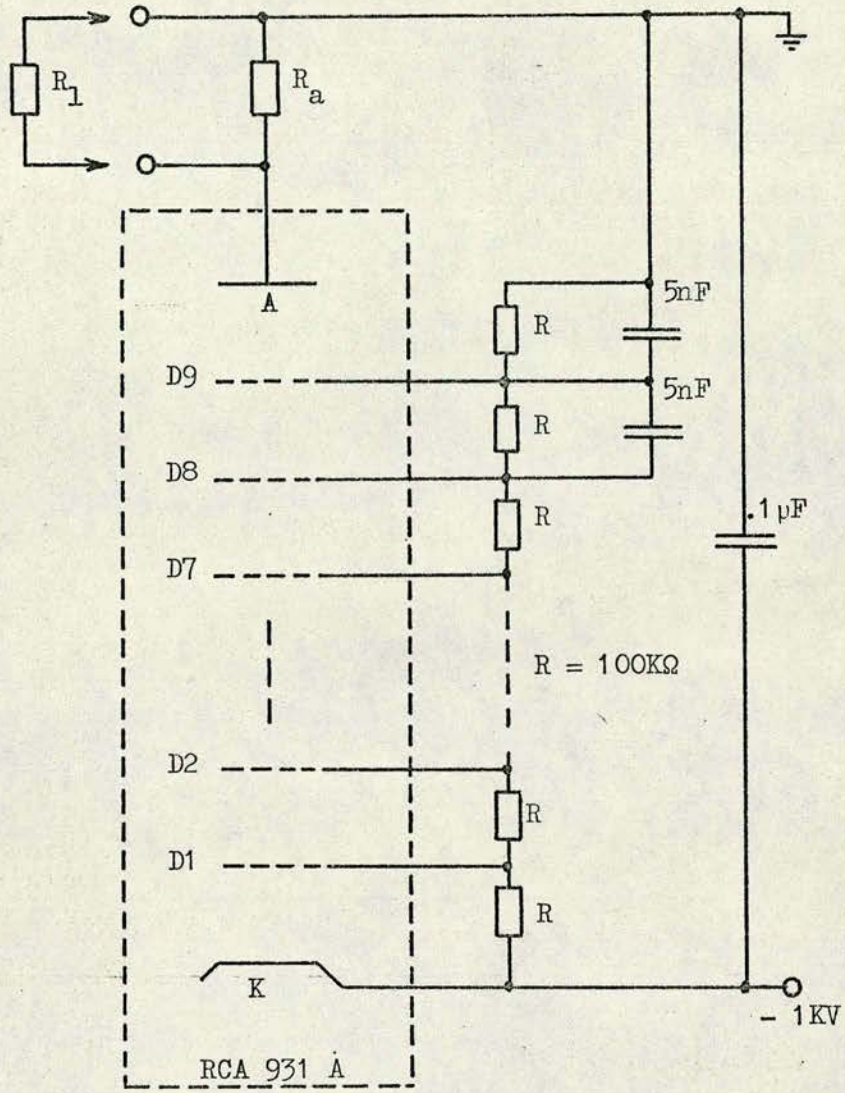

Fig. A7.1 Circuit diagram of the noise generator.

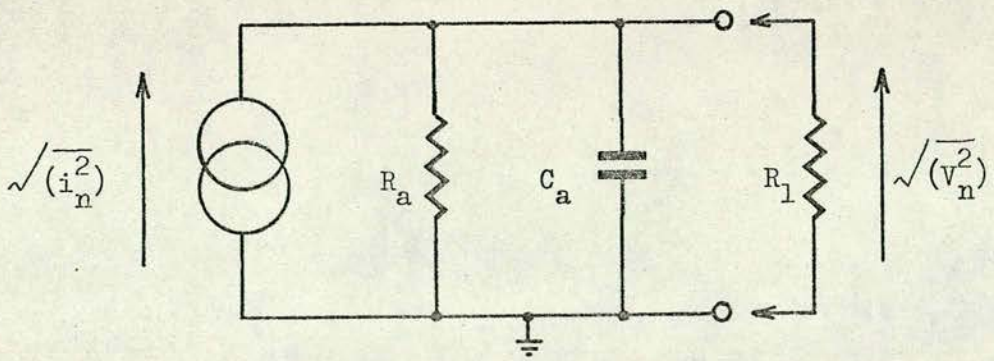

Fig. A7.2 Equivalent circuit of the noise generator.

The photo cathode of the PM is illuminated by a small 24-volt bulb. Since the light intensity produced by the bulb was found to be more than that required to give a d.c. anode current of 100 μA at the recommended supply voltage of - 1KV, a substantial area of the photo cathode is therefore masked and the bulb is run at a lower voltage (viz. approximately 12 volts).

For this application, the PM dynode voltages are required to be independent of the fluctuations in anode current. This is achieved (as shown) by a.c. decoupling the last two dynode stages where the fluctuations are likely to be large.

The a.c. equivalent circuit of the noise generator is shown in fig. A7.2. The thermal noise voltages produced by the anode resistance R_a and the load resistance R_l are omitted since they are very much smaller than the equivalent noise voltage produced by the PM. The anode-to-earth capacitance C_a together with R_a and R_l form a transfer characteristic which is low-pass in nature. However, for frequencies up to about 200 MHz, C_a was found to produce no appreciable shunting effect and may be neglected in this application accordingly.

For the RCA 931A device [83] used here, the overall gain of the 10-stage tube for a supply voltage of - 1KV is typically 8×10^5 giving a stage gain of 3.9. Consequently, with i_a = 100 μA, the expected mean square noise current per unit bandwidth is found [from equation (A7.1)] to be

$$\overline{i_n^2} = 3.4 \times 10^{-17} \quad [A]^2.H_z^{-1} \quad .....(A7.2).$$

For an r.f. noise bandwidth of about 1.5 MHz as in the experimental system (cf. chapter 5 below), then

$$\overline{i_n^2} = 5.1 \times 10^{-11} \quad [A]^2 \quad .....(A7.3),$$

so that $$\sqrt{(\overline{i_n^2})} \approx 7.2 \times 10^{-6} \quad [A] \quad .....(A7.4).$$

Accordingly, with $R_a = 1K\Omega$ and $R_1 = 10K\Omega$, then the r.m.s. noise voltage $\sqrt{(\overline{v_n^2})}$ appearing at the output of the noise generator is given approximately by

$$\sqrt{(\overline{v_n^2})} \approx 7.2 \times 0.91 \times 10^{-3} \approx 6.5 \quad [mV] \quad .....(A7.5)$$

This is the typical level of noise voltage found at the output of the PM noise generator. For experimental purposes, however, the noise-voltage level is readily controlled in two ways, viz.

(i) by varying the voltage on the light source in order to change the d.c. anode current of the PM, and

(ii) by varying the h.t. supply voltage in order to change the gain of the PM.

[Equation (A7.1) refers.]

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